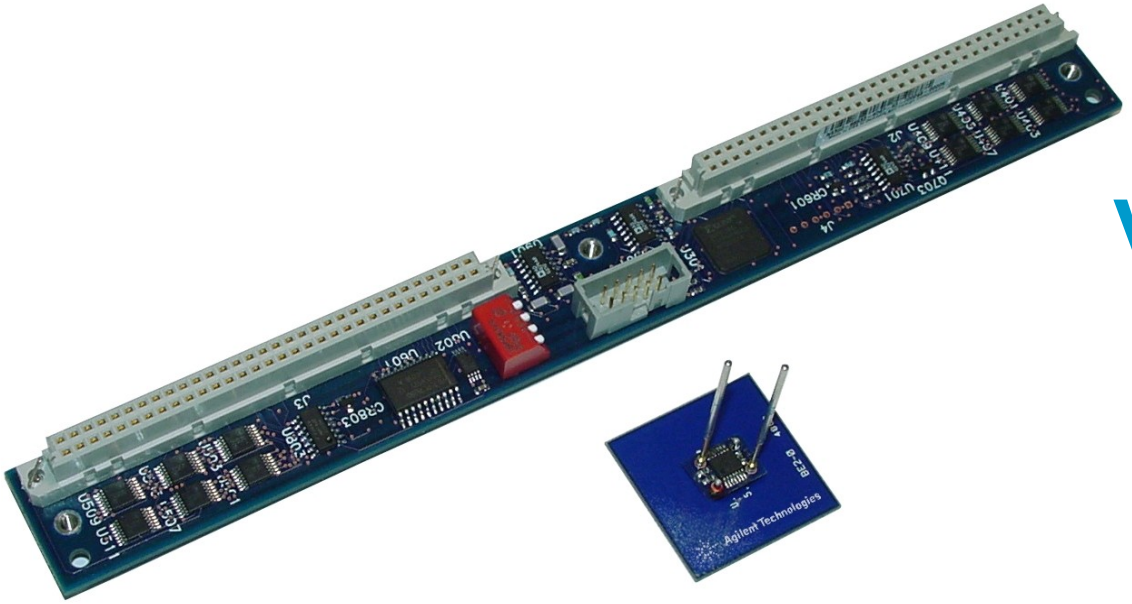
Austin User Group Meeting
ICT Update

January 2008

In-Circuit Test Agenda

- New Technology
- Software Revision 7.0 (i3070) Overview
- Software Revision 7.1 Overview
- Future Releases

Agilent Medalist i3070



VTEP v2.0

=

iVTEP

+

NPM

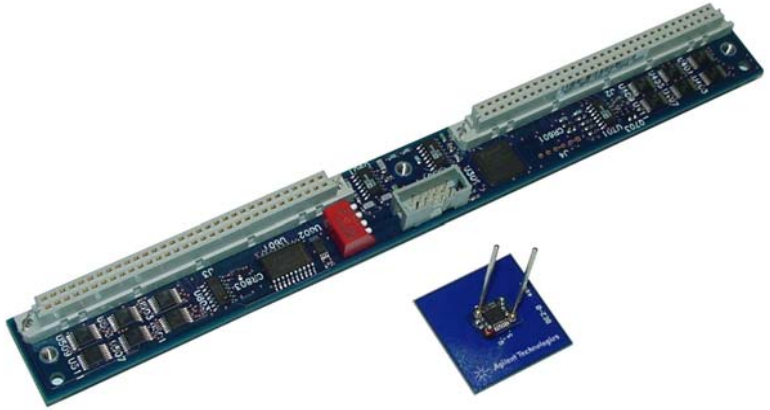
VTEP v2.0

	Devices (ICs)	Connectors	Sockets
VTEP			
iVTEP – ultra low signal pins			
NPM – power and grounds			7.1

VTEP v2.0 Hardware & Software

Hardware

Original VTEP hardware



Software

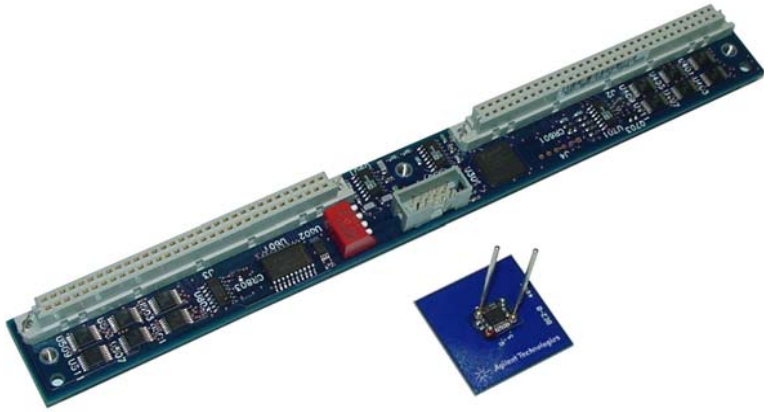
i3070 software (ver7.0)

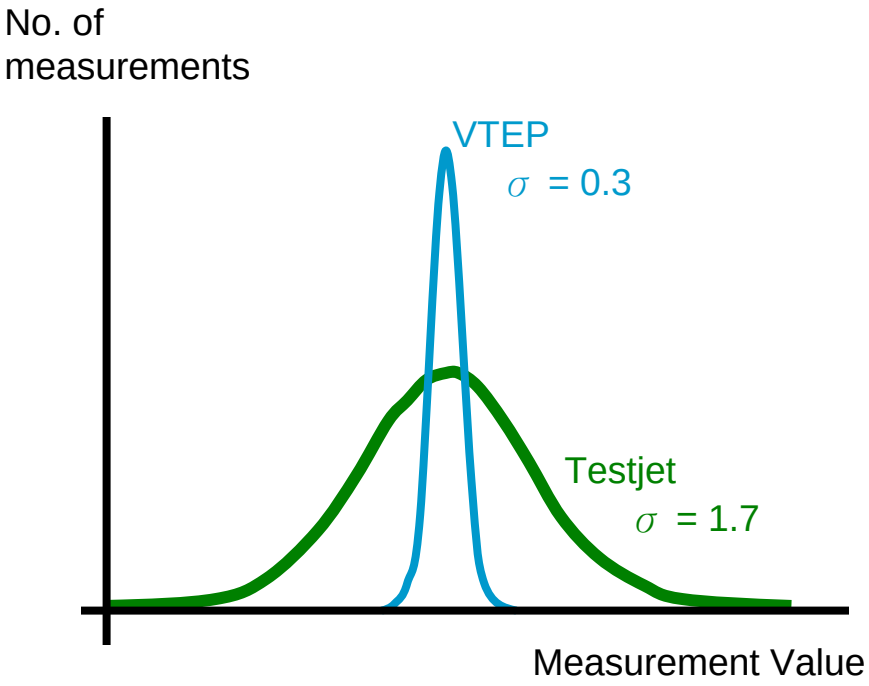
FREE* (no license needed)

* Available to all those on SUS contract

VTEP

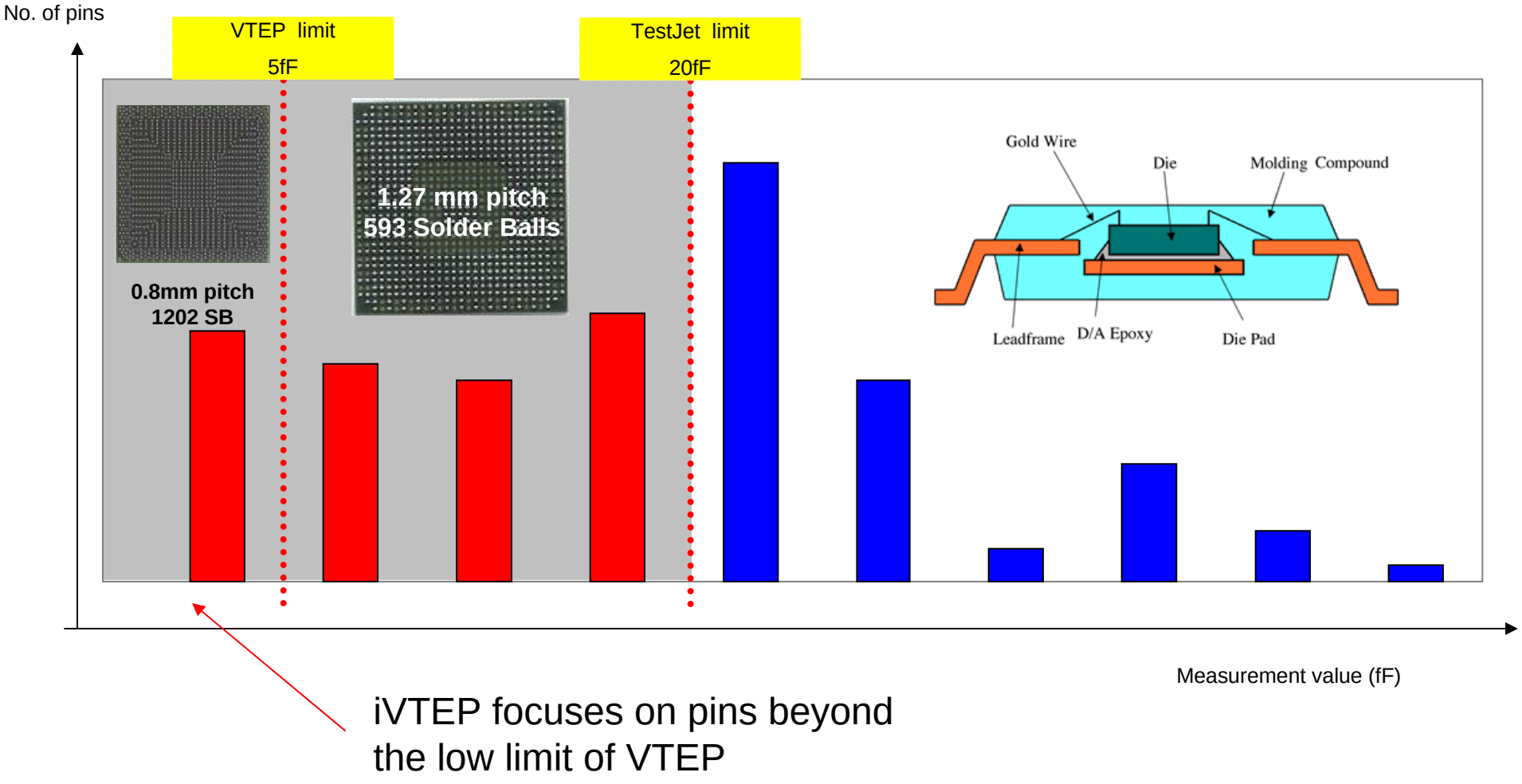
4X more sensitive
(from 20fF to 5fF)





5X better in standard deviation

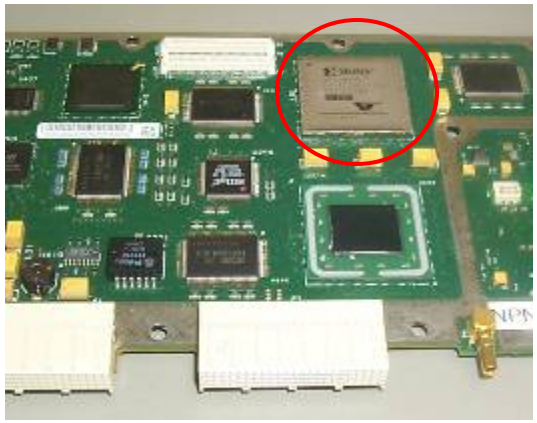
iVTEP

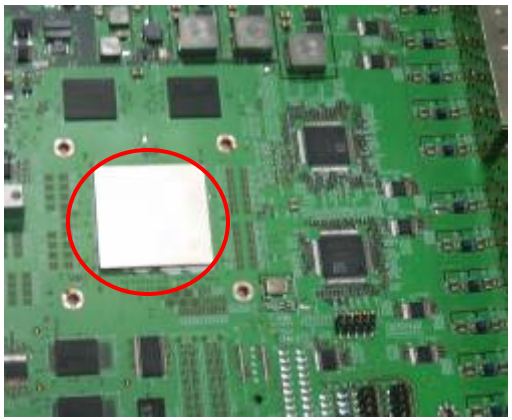


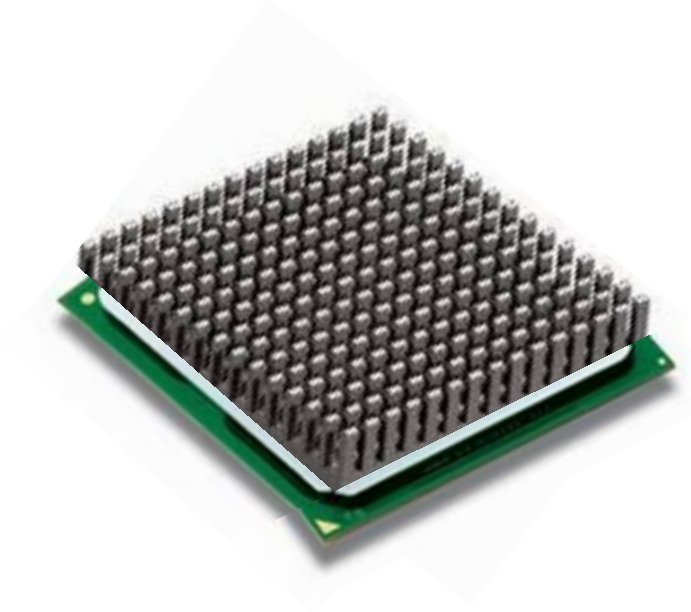
iVTEP focuses on pins beyond the low limit of VTEP

iVTEP target device

- Even works for ICs with heatspreaders and heatsinks



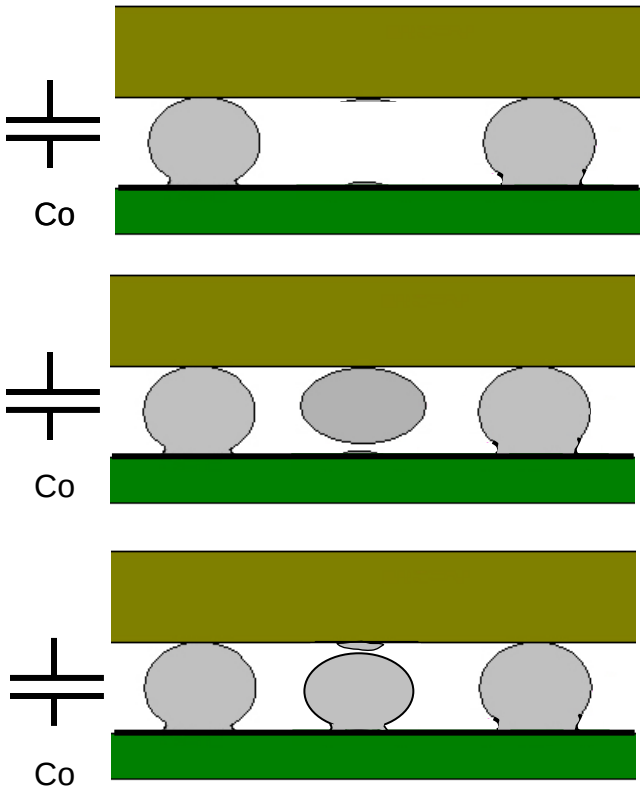




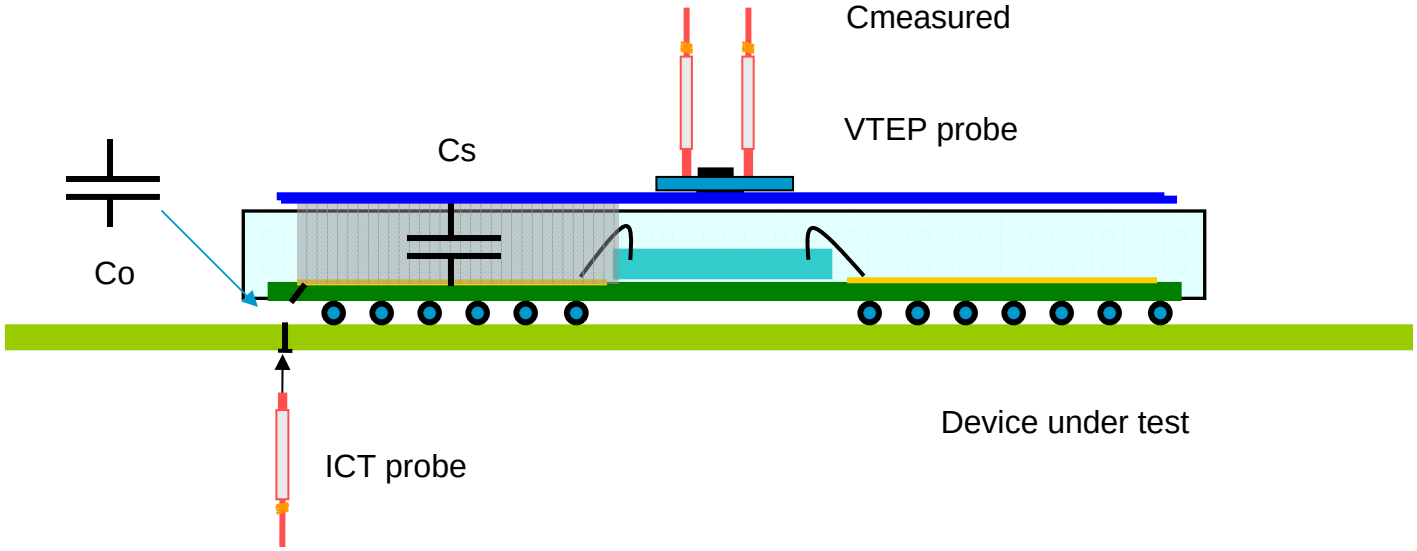
What happens when BGA is open?

- BGA opens are small capacitors (Co)
- Ideally, Co = eA/d where:
  - “e” = 8.84 fF/mm
  - “A” = area of pad/ball (mm^2)
  - “d” = distance between ball and pad (mm)
- Example: Missing 0.5 mm ball

Co = 8.84*(pi*(0.5mm/2)^2)/0.5mm = 3.5 fF

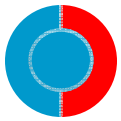


Detecting BGA opens with VTEP and iVTEP



- Cmeasured = CoCs/(Co + Cs)
- Example: Cs = 15fF, Co = 3.5fF

  Cmeasured = 15*3.5/(15 + 3.5) = 2.8 fF
- If a VTEP low threshold is set to 2, this defect will escape
- iVTEP will catch this.



NPM

Network Parameter Measurement

Sight beyond sight

Challenge

- Power and ground pins are not testable … until now.

- Proper grounding is crucial as High Speed Signal Propagation become more prevalent.

- PWR/GND makes up 35% - 45% of total pins

- Causes performance failure

- Only detectable at system test or not at all.

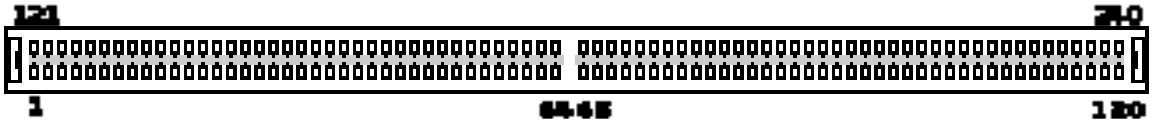
The solution

Network Parameter Measurement Technology:

- Detect and diagnose opens on power and ground pins.
- For connectors and sockets*
- Uses existing VTEP hardware
- FREE with ver7.0

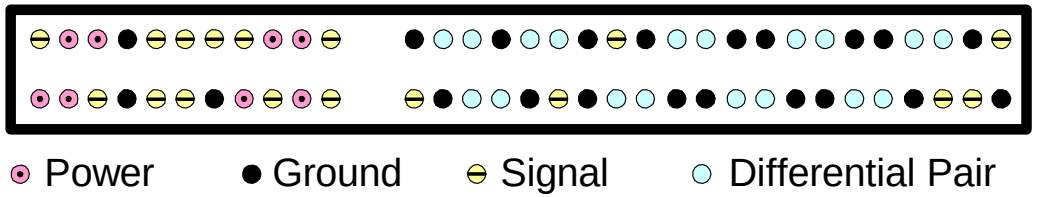
* Coverage on sockets is in the 7.1 release

Importance of power and ground



240 pin DIMM DDR2 connector > 88 out of 240 pins for power/ground

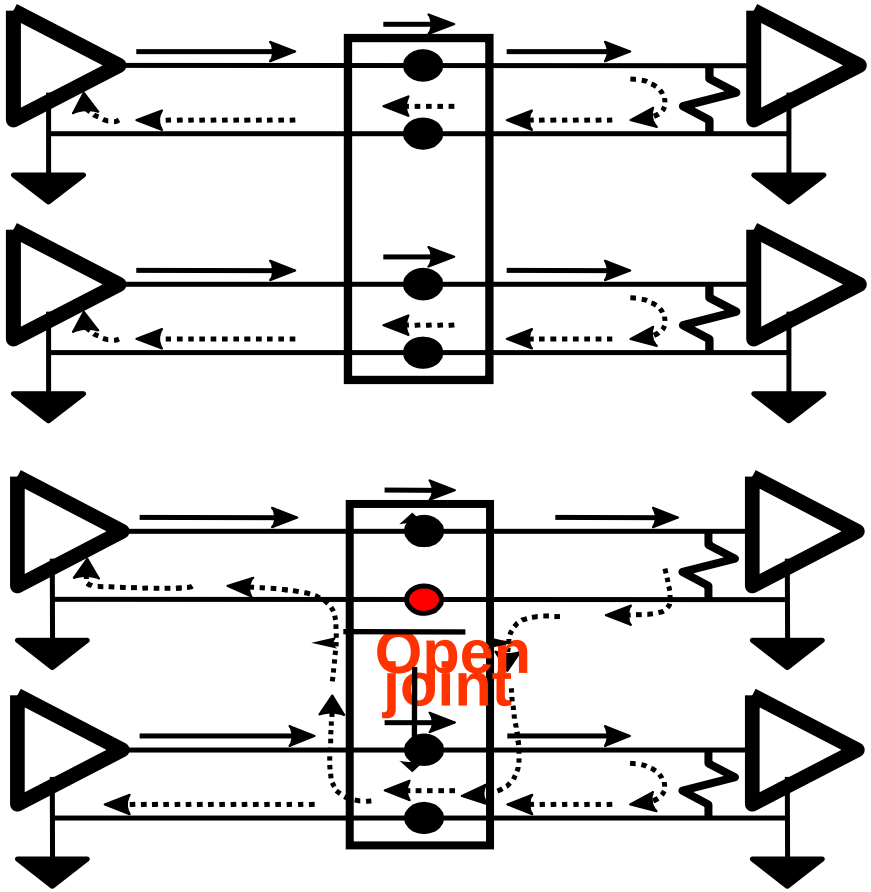
PCI Express x4 Connector Top View

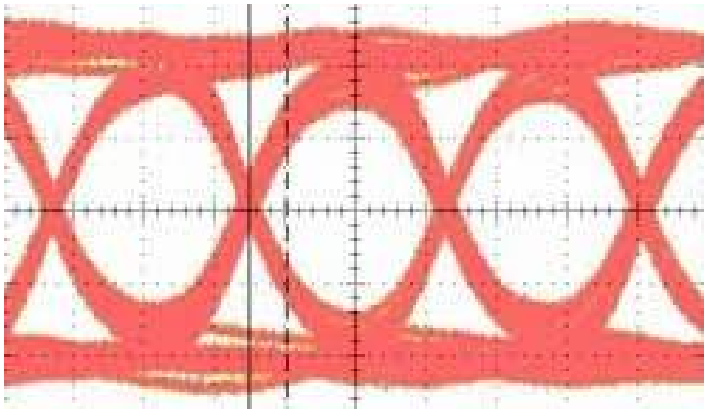


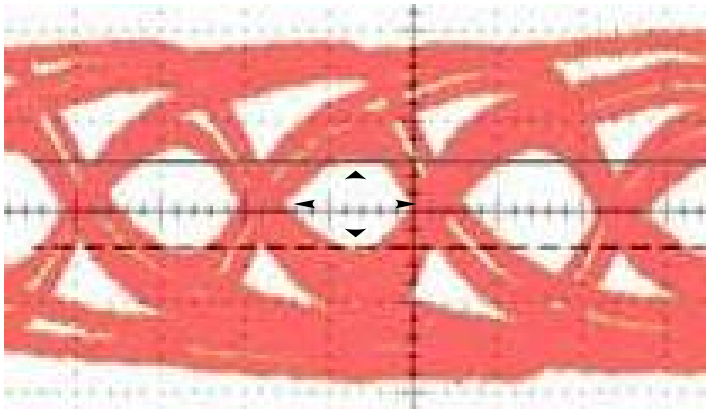
Power Ground Signal Differential Pair

PCI Express x4 connector > 29 out of 64 pins for power/ground

Network Parameter Measurement Technology : Industry challenges

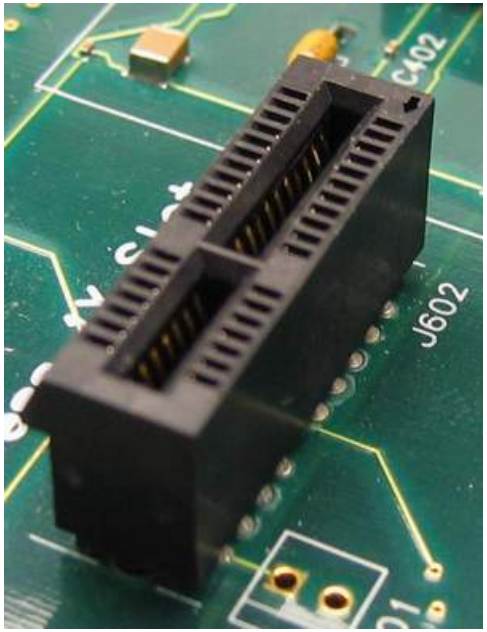




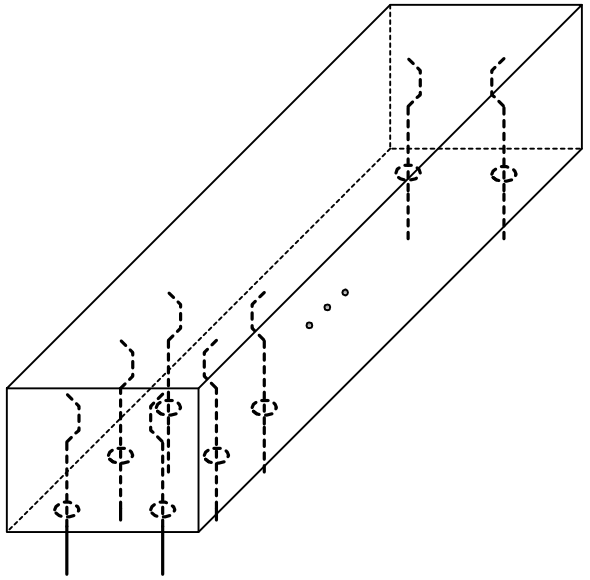


Degraded Eye Opening

The technology

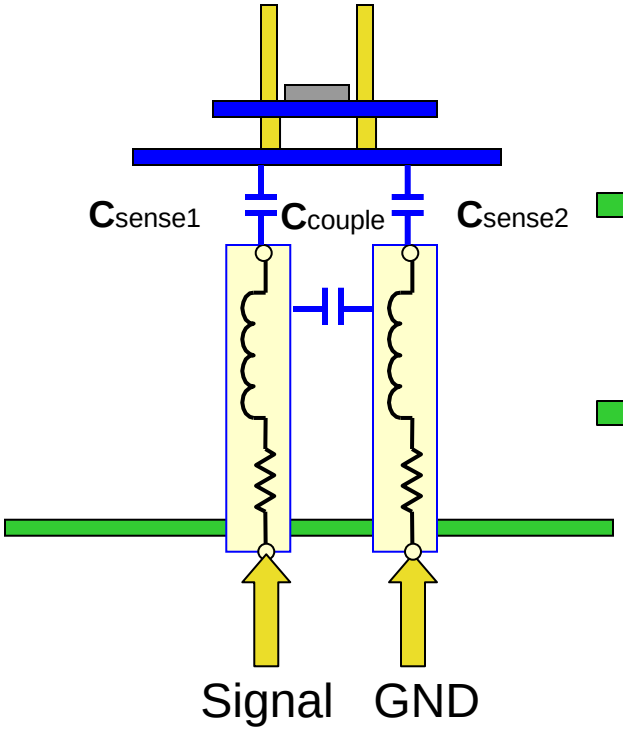


Network of Pins

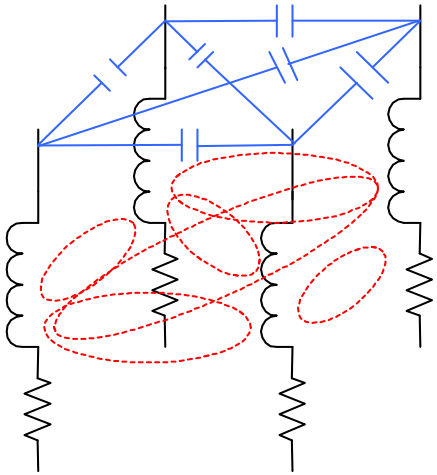


Network parameter measurement

Network Parameter Technology

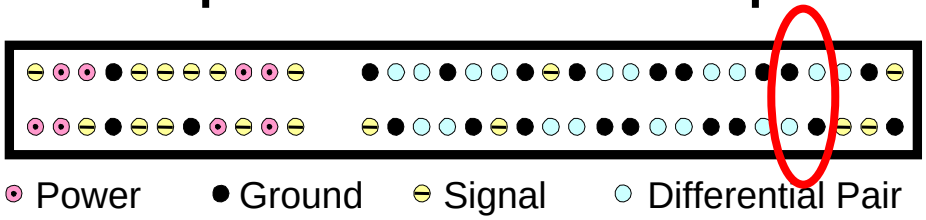


Sensor Plate capacitance



Spice Model

PCI Express x4 Connector Top View



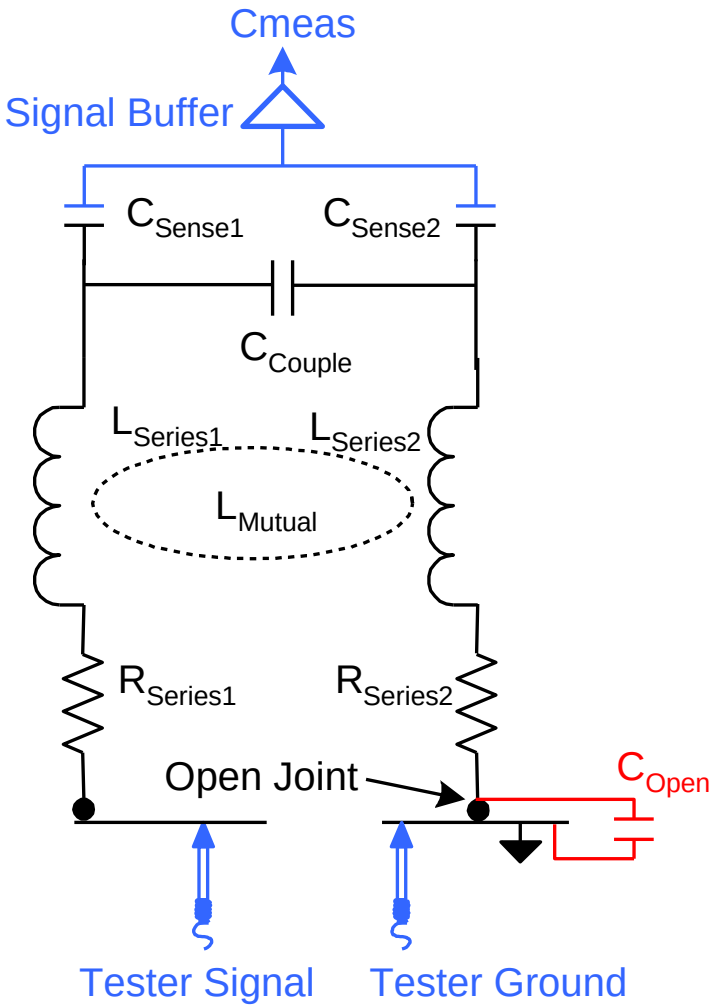
Network Parameter Technology – ITC paper

Submitted to ITC (do not copy)

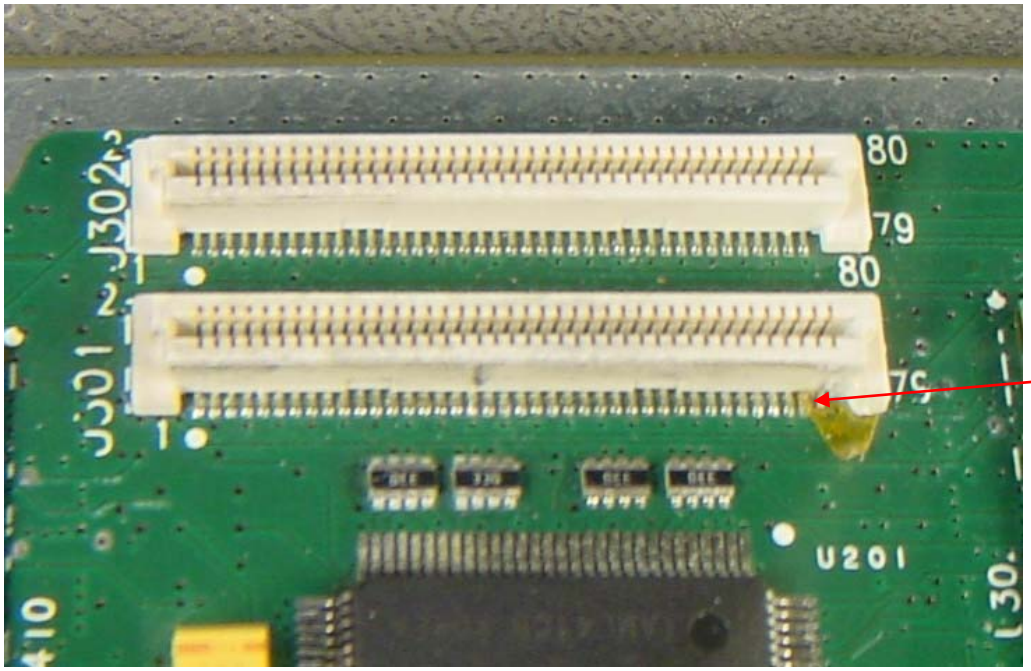
At VTEP measurement frequencies, inductance can be neglected. So can series resistance.

NPM works by examining the value of a good signal pin when there is a defect on an adjacent power or ground pin…

When a defect is present, the measured value of the signal pin increases, indicating a defect on the adjacent power or ground



Result




```
----------------------------------------
TestJet Report for "testjet_gx".
Tue Jan 02 15:40:02 2007
i3070 Demonstration Board
----------------------------------------
Open #1  Device j301
  Pin 75  Node GND
  Measured <NPM Open>
Open #2  Device j301
  Pin 79  Node GND
  Measured <NPM Open>
177983-3
----------------------------------------
```

Added ground defects to J301 – Caught as shown

VTEP v2.0 Benefits

Increased coverage

- Almost 100% Signal pin coverage on BGA
- Connector Power & Ground Pins

Uses existing VTEP H/W

FREE with software update (i3070)

Preserves high-speed signaling integrity

In-Circuit Test Agenda

- New Technology
- Software Revision 7.0 (i3070) Overview
- Software Revision 7.1 Overview
- Future Releases

The Next Generation ICT!
- Protects customer's investment

3070 Flexibility

i5000 Simplicity

Exciting new features

i3070 combines the flexibility of the 3070 tester with the ease of use features of the i5000, with new and improved capabilities and technologies.

***Medalist* i3070**

i3070 Rev 7.0 Key New Features

Increased test coverage

- VTEP v2.0
  - iVTEP (Award winning!)
  - Network Parameter Measurement

Time Saving Enhancements

- Test Algorithm Enhancements
- Time-To-Manufacturing improvements
  - AutoDebug Tool
  - AutoOptimizer Tool
  - Interactive Pin Locator Tool
- New Graphical User Interface (GUI)

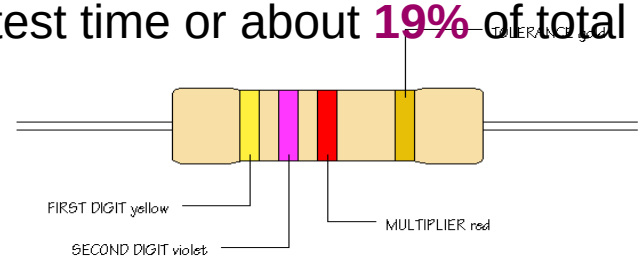
Compatibility

Increased Throughput Enhancements - Improved IPG!

New board tests generated with the new IPG will be f er!

Capacitor test improvements

- Improved IPG algorithm on frequency selection
  - Improved algorithm of Capacitor tests using fr1024
  - Select fr1024 instead of fr128 => reduce on “ed” measurements
  - Possible savings of about **48%** over total analog test time or about **19%** of total board test time

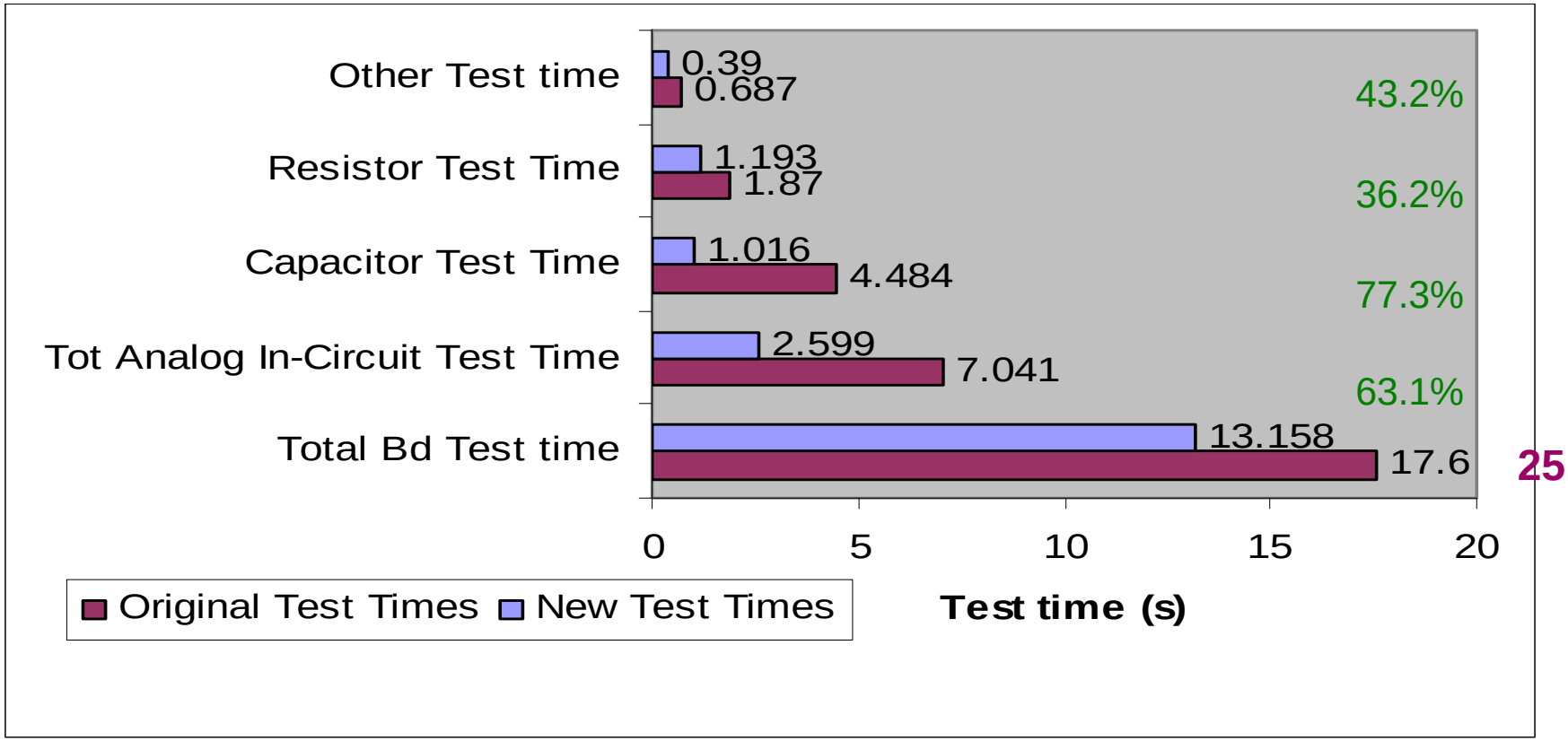


Resistor test improvements

- Adding of guarding to cancel capacitive impedance
- Recalculating wait time for capacitive charging
- Possible savings of about **9%** over total analog test time or about **3%** improvement over total board test time.

Increased Throughput Enhancements - Improved IPG!

Savings percent from test algorithm enhancements



*Savings over original test time %

Increased TTM Enhancements - Test Debug in Hours not Days

Shorts test improvements

- Minimisation of phantom shorts
  - Reorder nodes listing in shorts test
  - Reduction in Unpowered Test debug time.
  - Possible improvement of about half an hour for a board with 2000 nodes.

For a 2000 node board,		
Typical phantom shorts found	8	
Typical debug time required for each phantom shorts	10	min
	= 0.16	hrs
Typical debug time for phantom shorts	1.3	hrs
Typical debug time for shorts test	2	days
	= 16	hrs
Possible minimisation of phantom shorts	4	
Typical savings	**0.67**	**hrs**
Typical savings over total shorts debug time %	**4.2**	**%**

Increased TTM Enhancements - Test Debug in Hours not Days

AutoDebug

- First introduced in i5000
- Debugs analog tests at the click of a button
- Uses a set of user definable rules
- Uses statistical methods to determine test stability
- Analog test debug typically reduced from **2days to 4hours**

Increased Throughput
- Improvement in Efficiency

AutoOptimizer

- Removes excessive test options that take up test time
- Optimises test times to initial debugged state
- Uses statistical methods (CPK, user definable) to determine stability of test

AutoOptimizer	**A**	**B**	**C**	**D**	**E**	**F**
Number of Analog tests	54	60	101	109	140	1968
Test Time-analog only	0.77s	0.78s	2.42s	1.07s	2.41s	26.7s
Optimised Time-analog only	0.38s	0.45s	1.72s	0.83s	1.73s	22.6s
Improvement %	**51.0%**	**42.0%**	**29.0%**	**20.9%**	**28.0%**	***15.3%**

*Note that this time savings was achieved even after user manually optimised the test.

Interactive Pin Locator

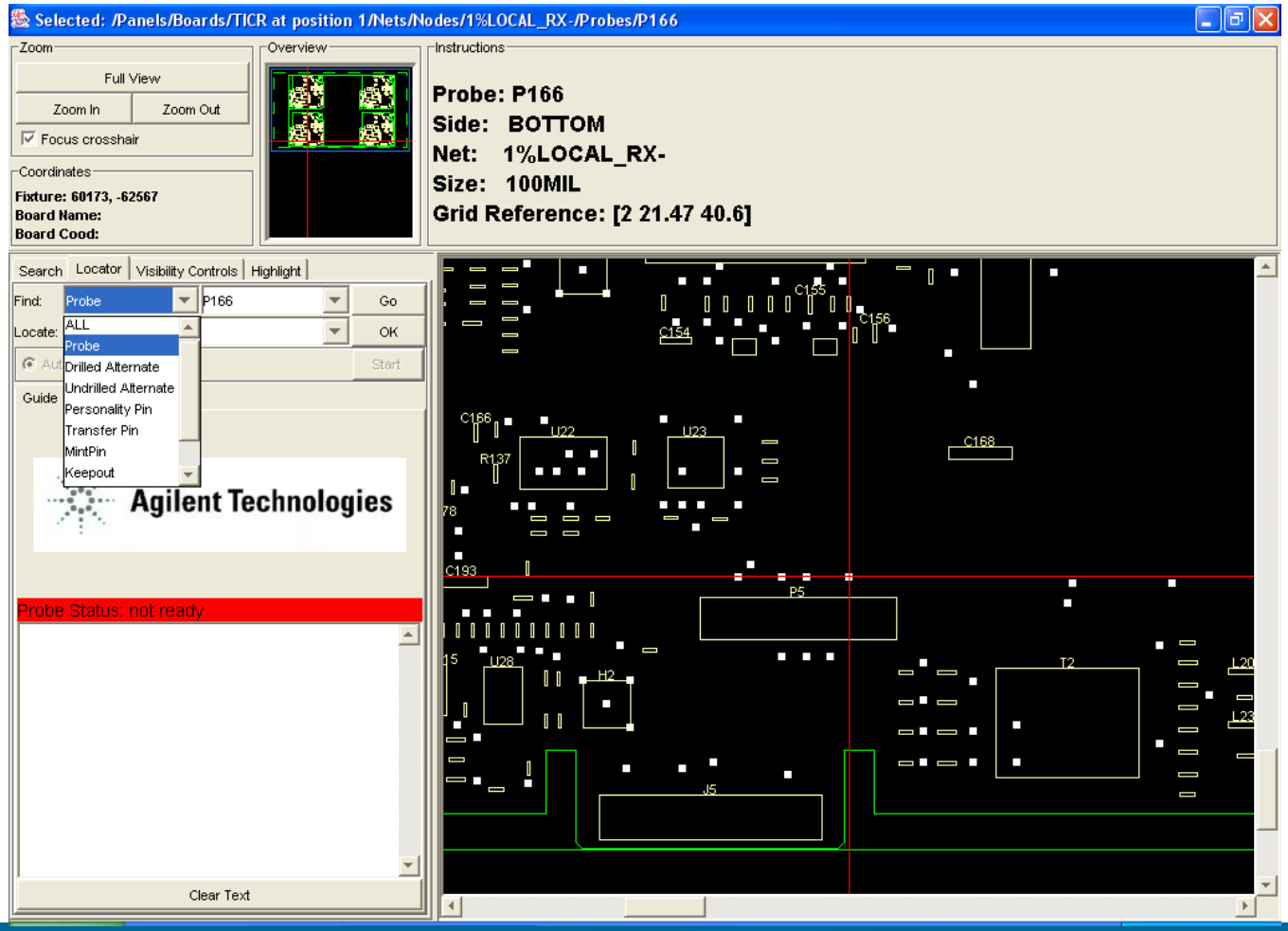
A new tool to similar to the “find pins” feature on the 3070, with lots of enhancements!

- This is a graphical “find pins”
- It indicates the location of the node that you are finding and interactively displays an arrow from where you have placed the manual probe to the target pin/probe.
- This tool really shortens the time needed to find a probe on the fixture. It is particularly useful when debugging tests or finding the “Worst Probe” during production testing.
- **Gone are the days when you have to find the probe/pin based on the BBRRCC!**

Increased TTM Enhancements - Test Debug in Hours not Days

Interactive Pin Locator

Gone are the days when you have to find the probe/pin based on the BBRRCC!

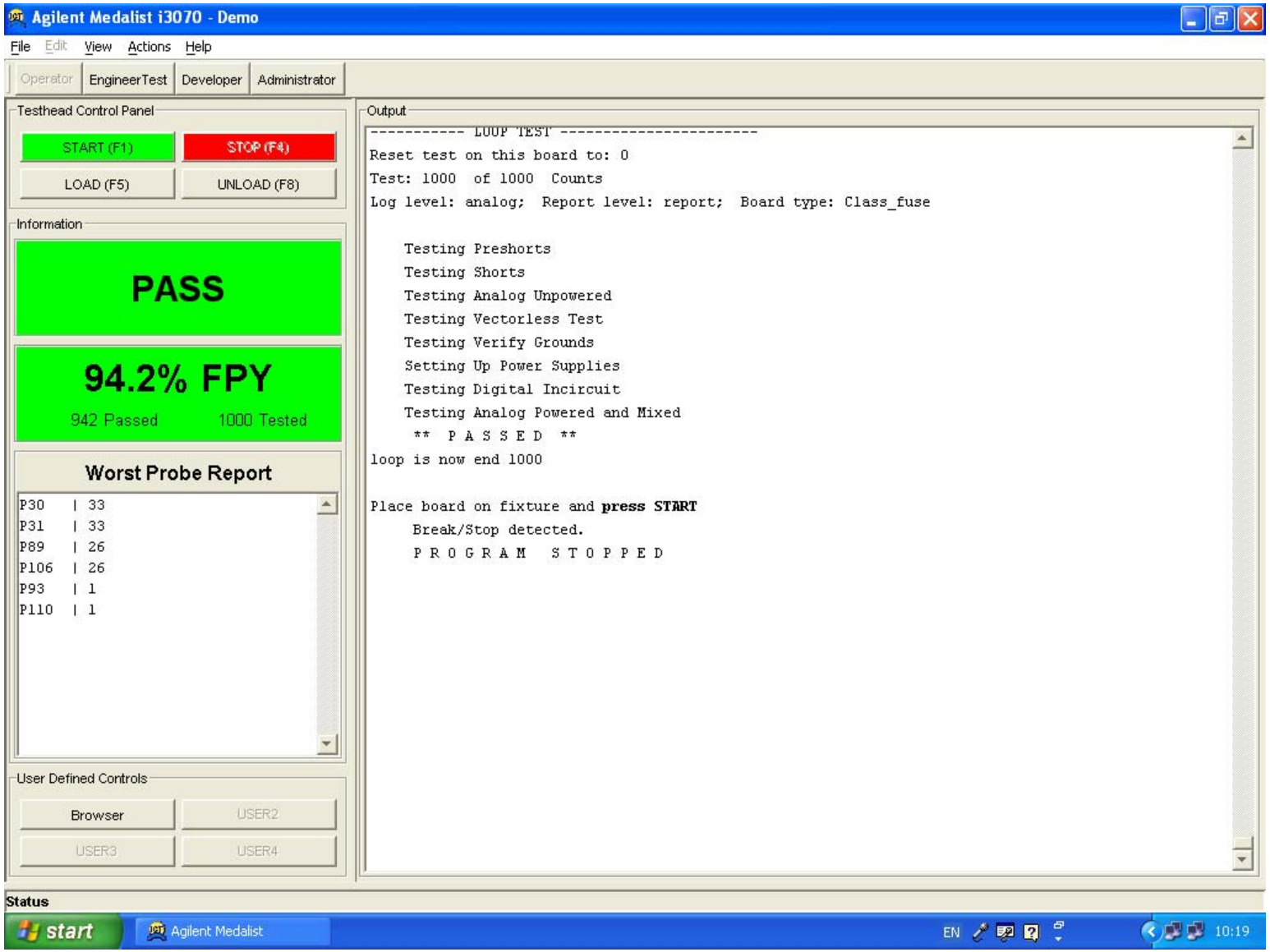


New, Easy to Use
- Graphical User Interface

- Windows-based familiarity
  - Simple point and click interface
- Different Operator Logins for test code security
  - Operator Login
  - Engineer Login
  - Administrator Login
- Worst Probe Reports and Yield Reports
- Analog test Autodebug and AutoOptimiser
  - Auto-debug or Optimise analog tests with just one click

Graphical User Interface

Operator Login

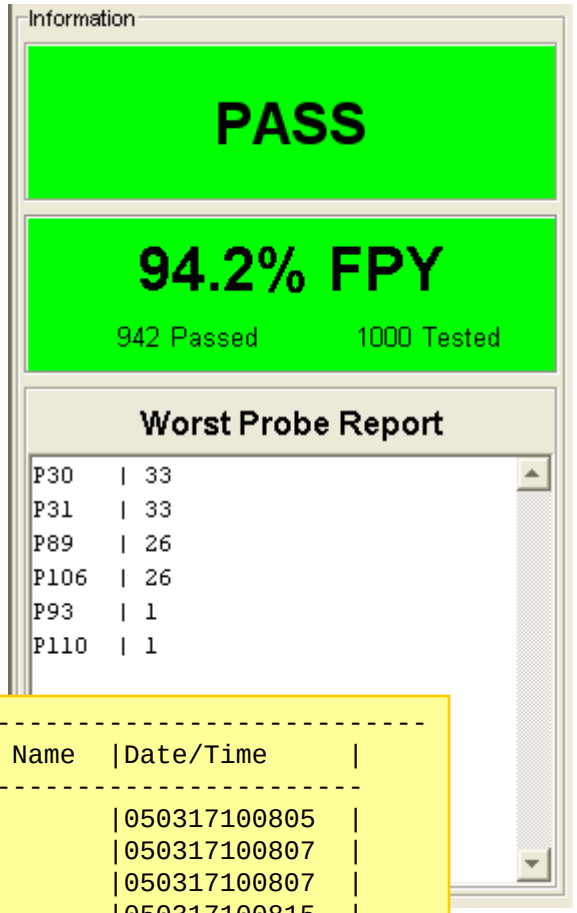


Graphical User Interface

Worst Probe Report

Shows the most common probes that are found in failed tests

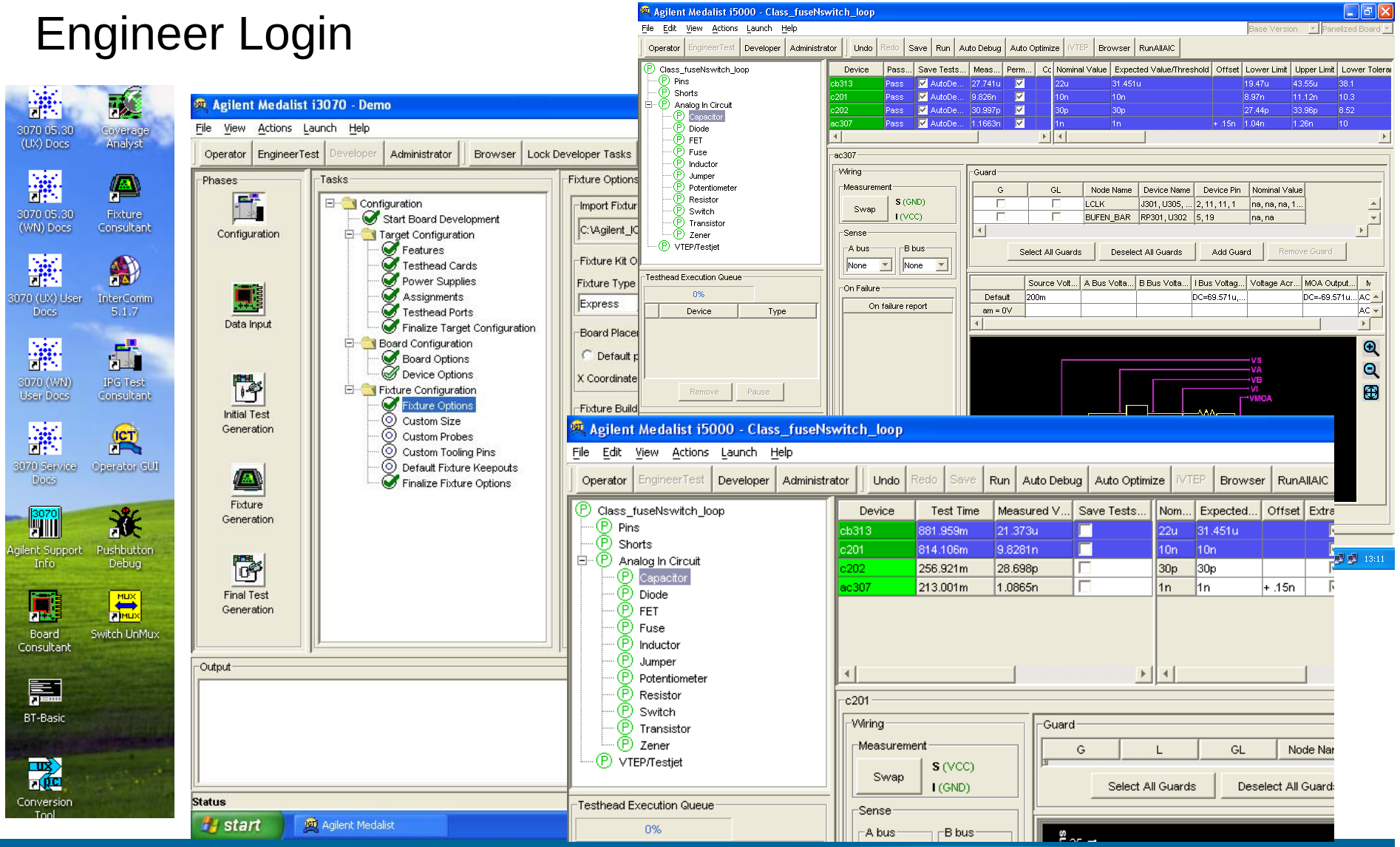
It can be disabled (if necessary)



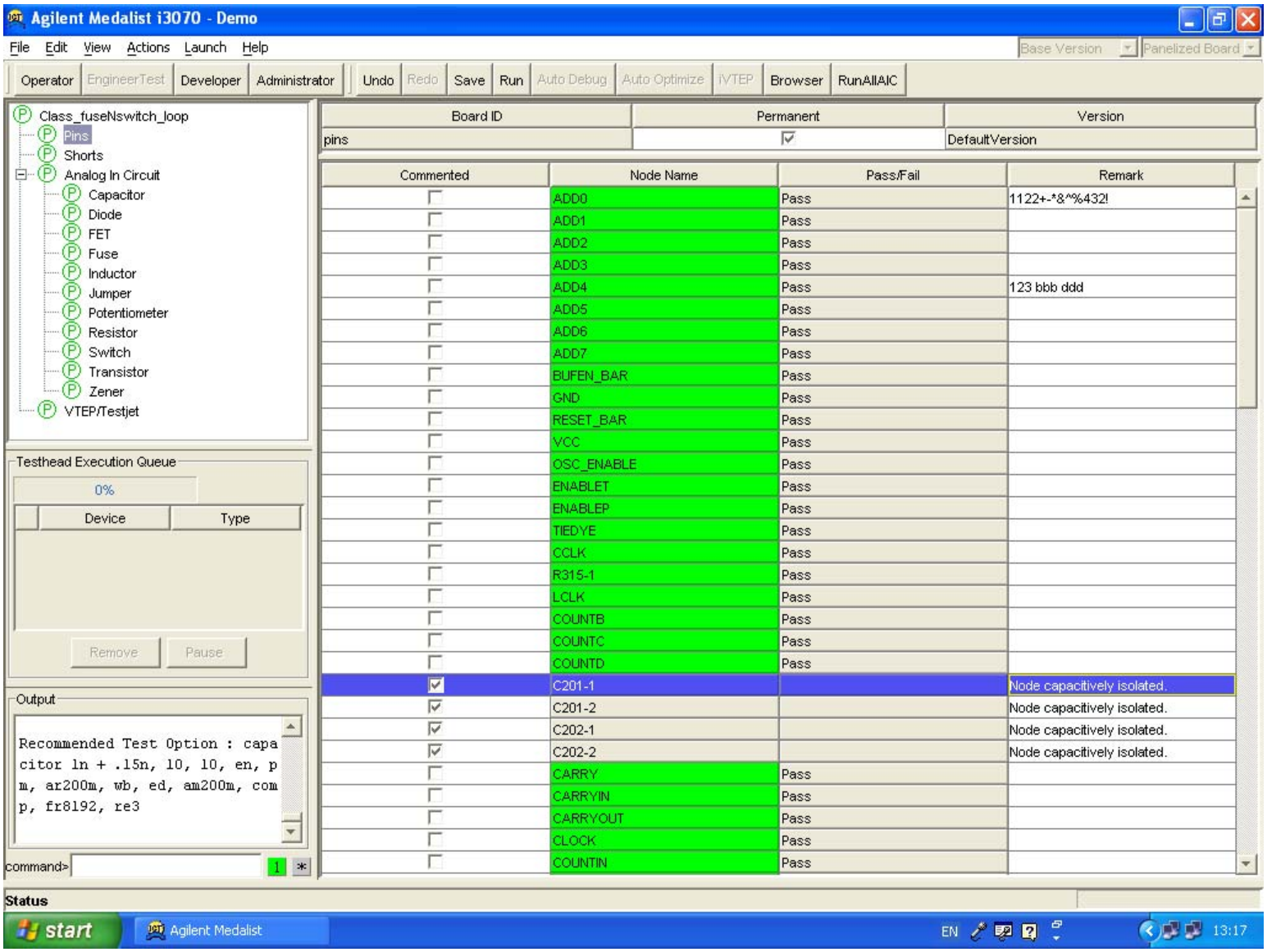
Failure type	Probe	Usage	Node Name	Device Name	Date/Time
Shorts Failure	P223	1	/U205-13	tp605	050317100805
Analog Failure	P50	1	/EEPROM_CLK	tp656	050317100807
Analog Failure	P296	1	DCOM	tp787	050317100807
Shorts Failure	P223	1	/U205-13	tp605	050317100815
Analog Failure	P50	1	/EEPROM_CLK	tp656	050317100817
Analog Failure	P296	1	DCOM	tp787	050317100817

Graphical User Interface

Engineer Login



Engineer Login



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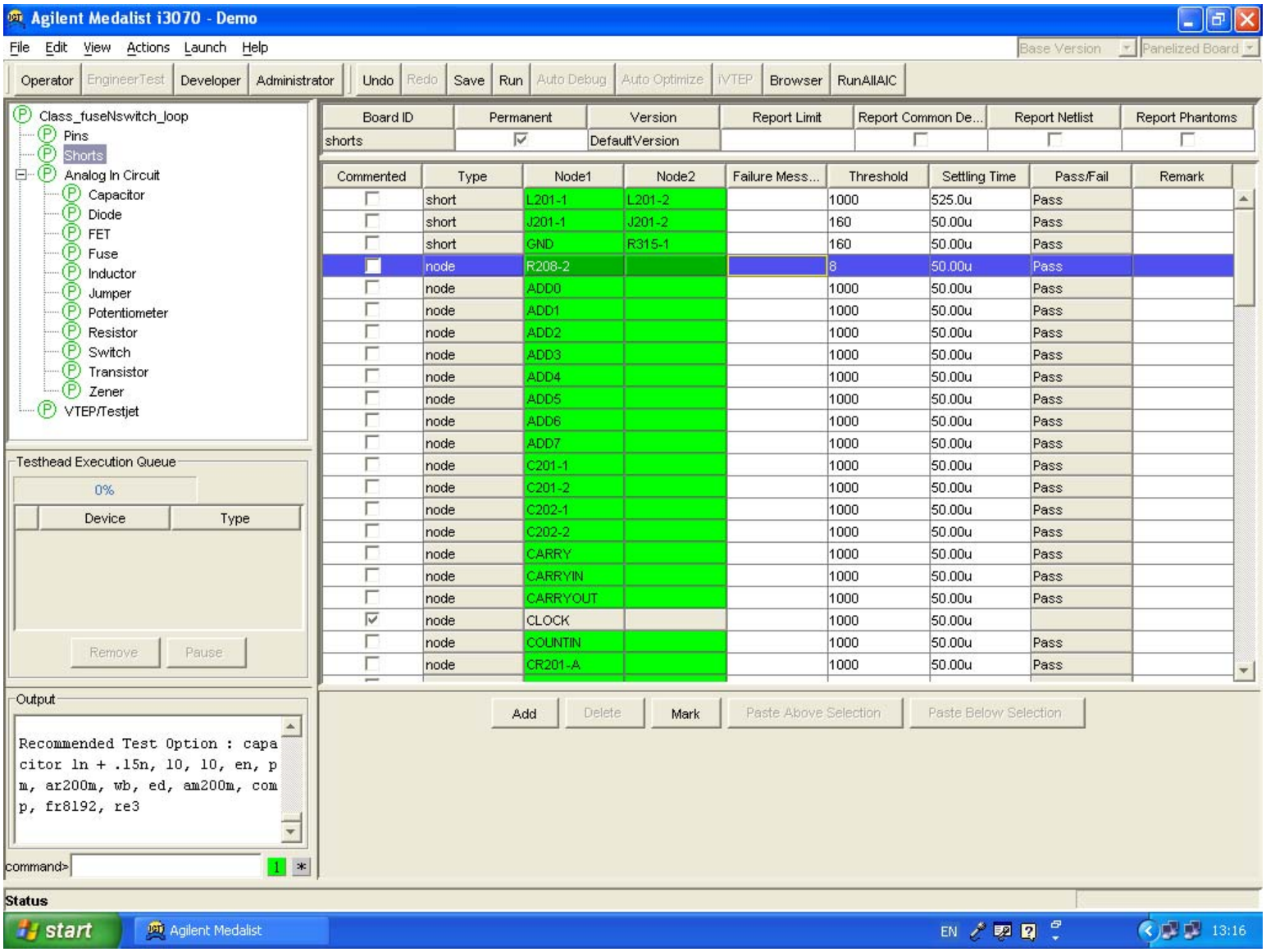
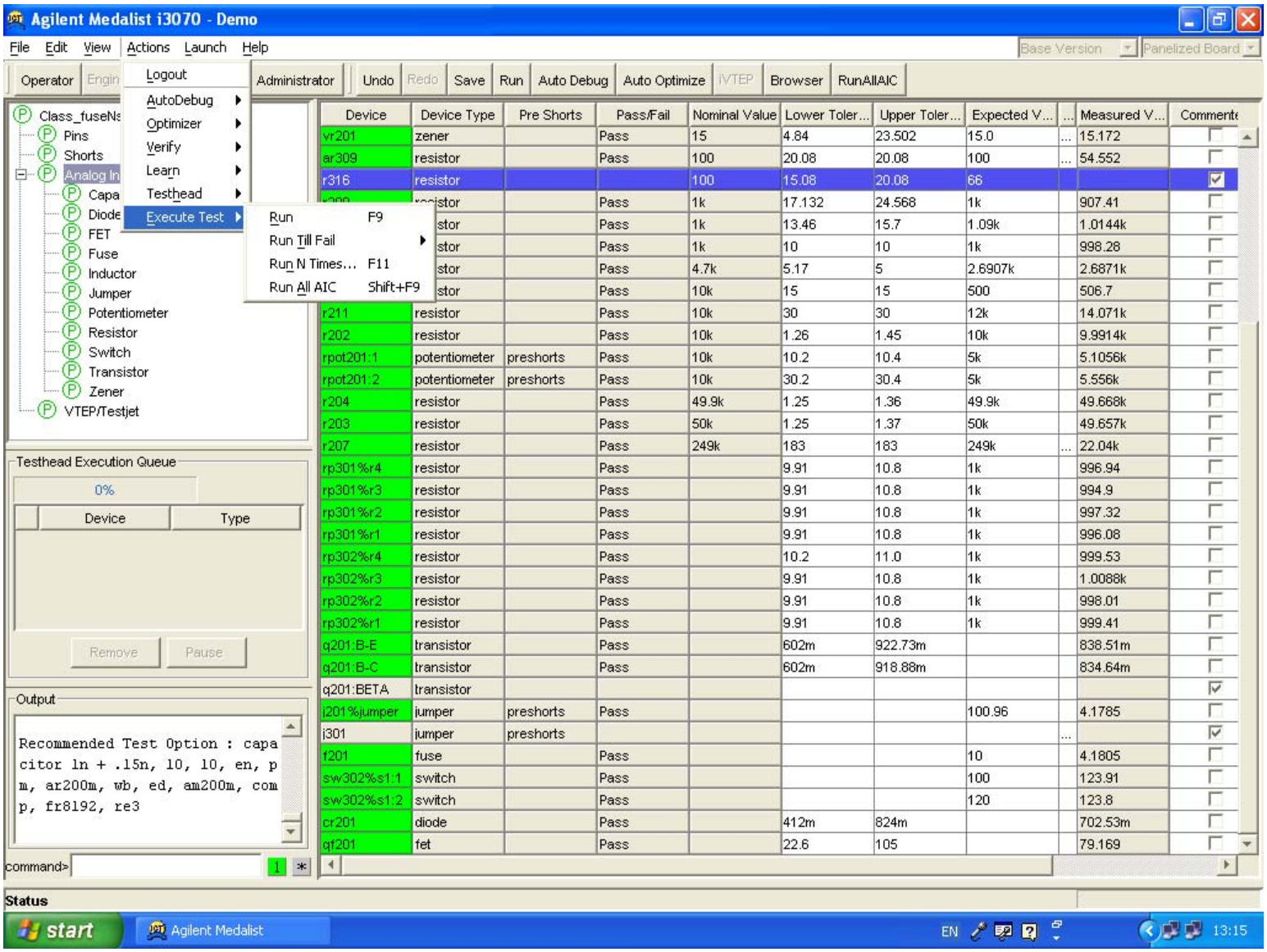
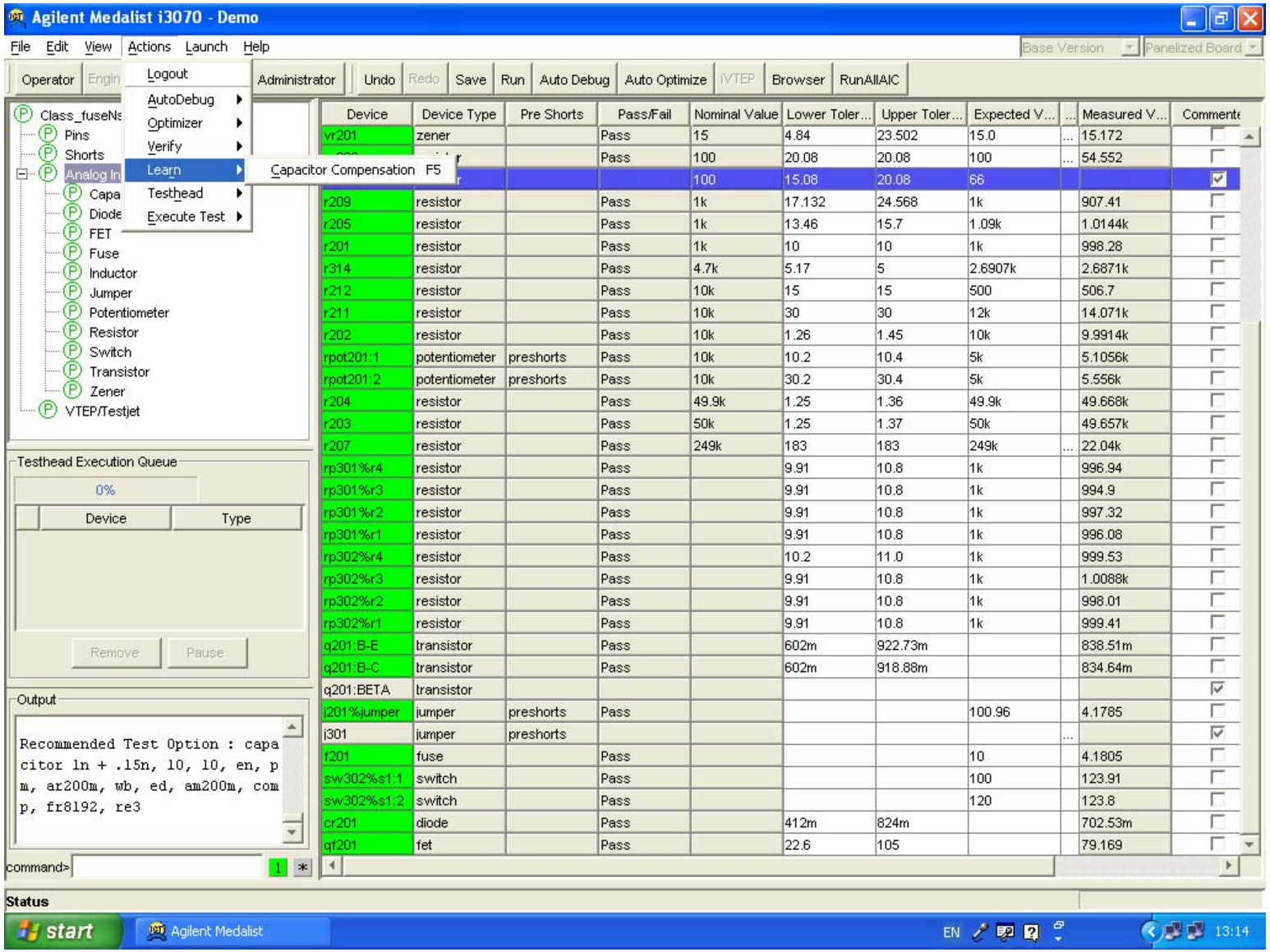


Engineer Login

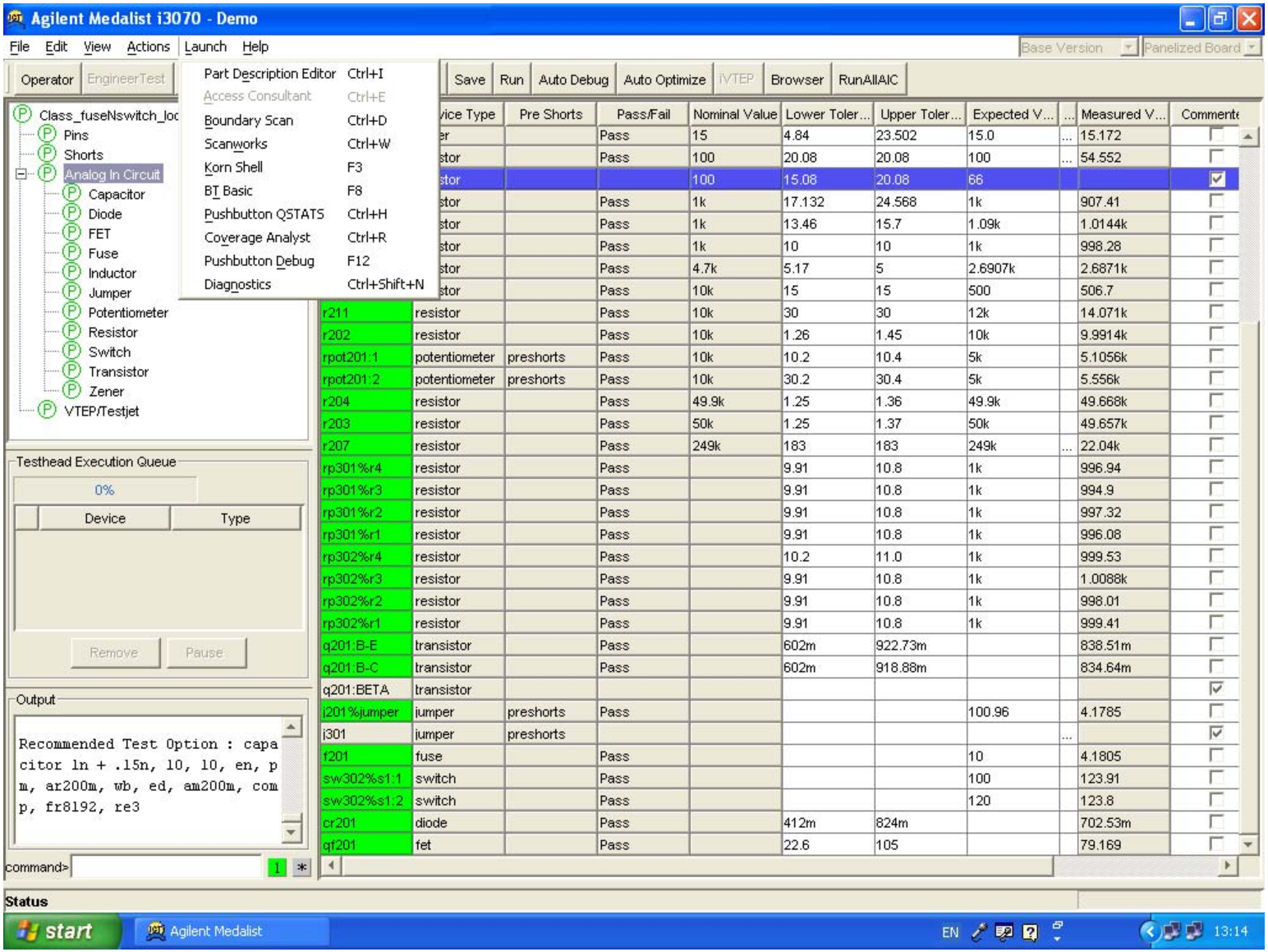


Engineer Login



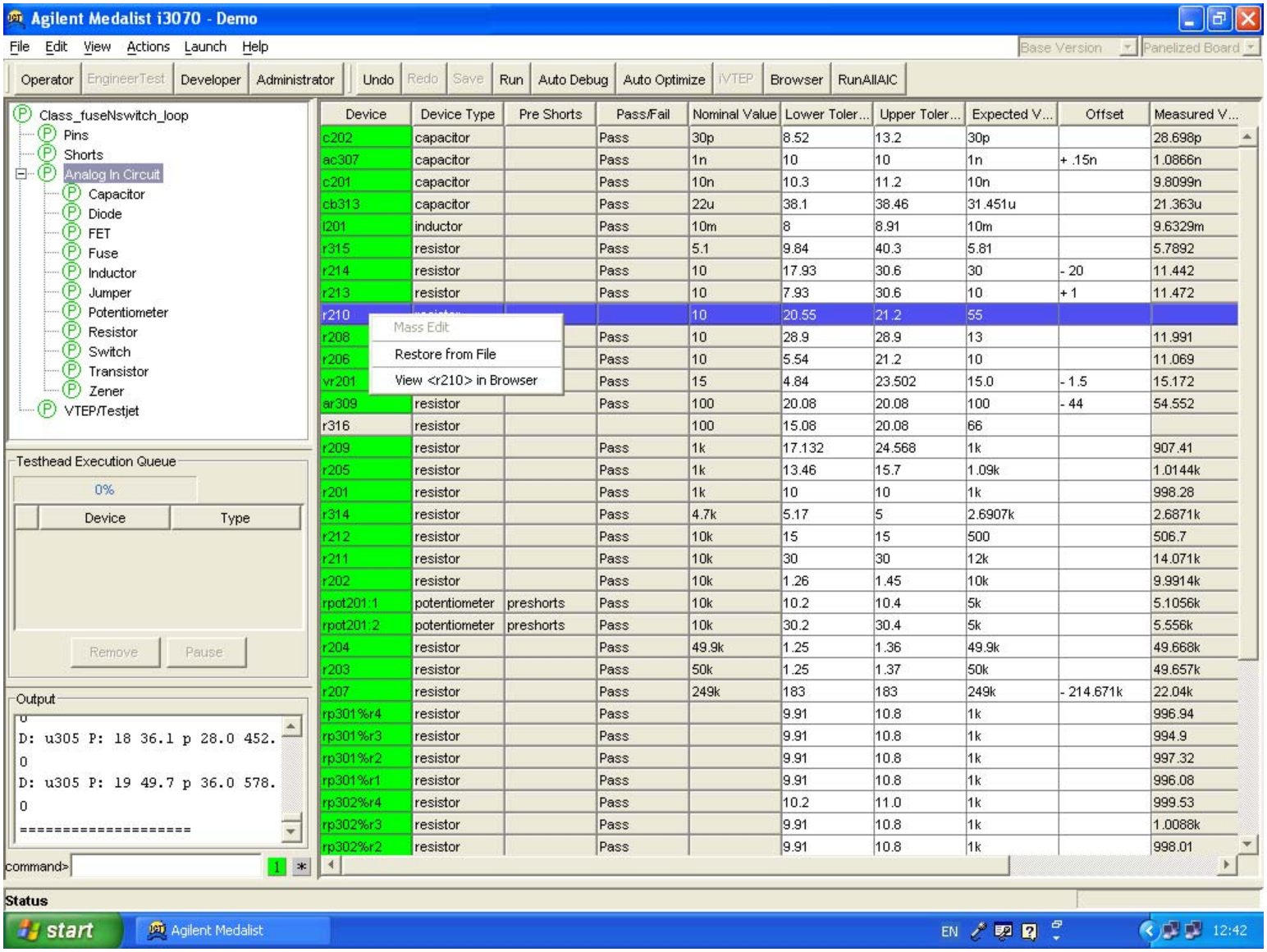
Device	Device Type	Pre Shorts	Pass/Fail	Nominal Value	Lower Toler...	Upper Toler...	Expected V...	...	Measured V...	Comment
vr201	zener		Pass	15	4.84	23.502	15.0	...	15.172	
			Pass	100	20.08	20.08	100	...	54.552	
				100	15.08	20.08	66			
r209	resistor		Pass	1k	17.132	24.568	1k		907.41	
r205	resistor		Pass	1k	13.46	15.7	1.09k		1.0144k	
r201	resistor		Pass	1k	10	10	1k		998.28	
r314	resistor		Pass	4.7k	5.17	5	2.6907k		2.6871k	
r212	resistor		Pass	10k	15	15	500		506.7	
r211	resistor		Pass	10k	30	30	12k		14.071k	
r202	resistor		Pass	10k	1.26	1.45	10k		9.9914k	
rpot201:1	potentiometer	preshorts	Pass	10k	10.2	10.4	5k		5.1056k	
rpot201:2	potentiometer	preshorts	Pass	10k	30.2	30.4	5k		5.556k	
r204	resistor		Pass	49.9k	1.25	1.36	49.9k		49.668k	
r203	resistor		Pass	50k	1.25	1.37	50k		49.657k	
r207	resistor		Pass	249k	183	183	249k	...	22.04k	
rp301%r4	resistor		Pass		9.91	10.8	1k		996.94	
rp301%r3	resistor		Pass		9.91	10.8	1k		994.9	
rp301%r2	resistor		Pass		9.91	10.8	1k		997.32	
rp301%r1	resistor		Pass		9.91	10.8	1k		996.08	
rp302%r4	resistor		Pass		10.2	11.0	1k		999.53	
rp302%r3	resistor		Pass		9.91	10.8	1k		1.0088k	
rp302%r2	resistor		Pass		9.91	10.8	1k		998.01	
rp302%r1	resistor		Pass		9.91	10.8	1k		999.41	
q201:B-E	transistor		Pass		602m	922.73m			838.51m	
q201:B-C	transistor		Pass		602m	918.88m			834.64m	
q201:BETA	transistor									
j201%jumper	jumper	preshorts	Pass				100.96		4.1785	
j301	jumper	preshorts						...		
f201	fuse		Pass				10		4.1805	
sw302%s1:1	switch		Pass				100		123.91	
sw302%s1:2	switch		Pass				120		123.8	
cr201	diode		Pass		412m	824m			702.53m	
qf201	fet		Pass		22.6	105			79.169	

Engineer Login

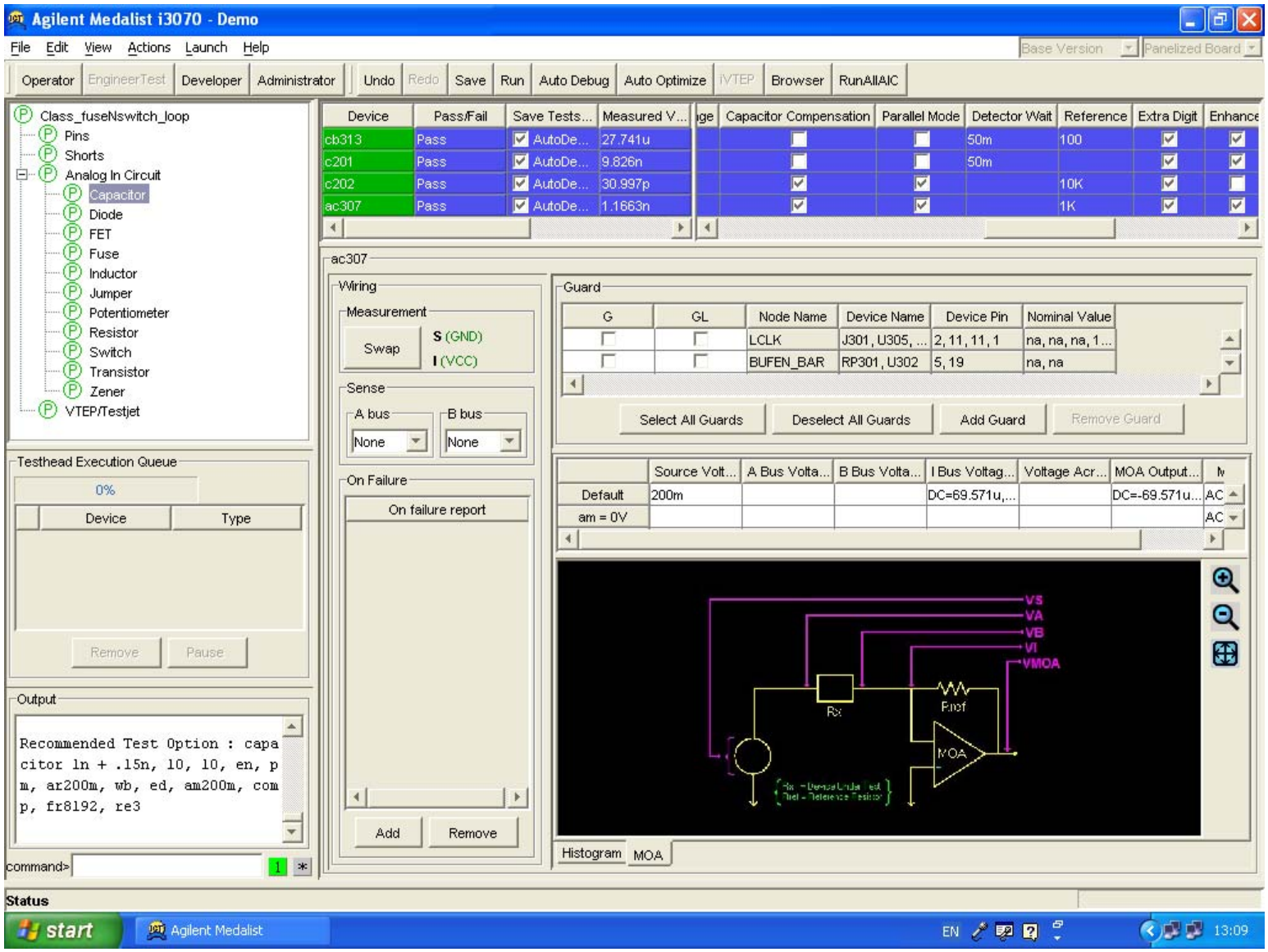


	vice Type	Pre Shorts	Pass/Fail	Nominal Value	Lower Toler...	Upper Toler...	Expected V...	...	Measured V...	Comment
	er		Pass	15	4.84	23.502	15.0	...	15.172	
	stor		Pass	100	20.08	20.08	100	...	54.552	
	stor			100	15.08	20.08	66			☑
	stor		Pass	1k	17.132	24.568	1k		907.41	
	stor		Pass	1k	13.46	15.7	1.09k		1.0144k	
	stor		Pass	1k	10	10	1k		998.28	
	stor		Pass	4.7k	5.17	5	2.6907k		2.6871k	
	stor		Pass	10k	15	15	500		506.7	
r211	resistor		Pass	10k	30	30	12k		14.071k	
r202	resistor		Pass	10k	1.26	1.45	10k		9.9914k	
rpot201:1	potentiometer	preshorts	Pass	10k	10.2	10.4	5k		5.1056k	
rpot201:2	potentiometer	preshorts	Pass	10k	30.2	30.4	5k		5.556k	
r204	resistor		Pass	49.9k	1.25	1.36	49.9k		49.668k	
r203	resistor		Pass	50k	1.25	1.37	50k		49.657k	
r207	resistor		Pass	249k	183	183	249k	...	22.04k	
rp301%r4	resistor		Pass		9.91	10.8	1k		996.94	
rp301%r3	resistor		Pass		9.91	10.8	1k		994.9	
rp301%r2	resistor		Pass		9.91	10.8	1k		997.32	
rp301%r1	resistor		Pass		9.91	10.8	1k		996.08	
rp302%r4	resistor		Pass		10.2	11.0	1k		999.53	
rp302%r3	resistor		Pass		9.91	10.8	1k		1.0088k	
rp302%r2	resistor		Pass		9.91	10.8	1k		998.01	
rp302%r1	resistor		Pass		9.91	10.8	1k		999.41	
q201:B-E	transistor		Pass		602m	922.73m			838.51m	
q201:B-C	transistor		Pass		602m	918.88m			834.64m	
q201:BETA	transistor									☑
j201%jumper	jumper	preshorts	Pass				100.96		4.1785	
j301	jumper	preshorts						...		☑
f201	fuse		Pass				10		4.1805	
sw302%s1:1	switch		Pass				100		123.91	
sw302%s1:2	switch		Pass				120		123.8	
cr201	diode		Pass		412m	824m			702.53m	
qf201	fet		Pass		22.6	105			79.169	

Engineer Login

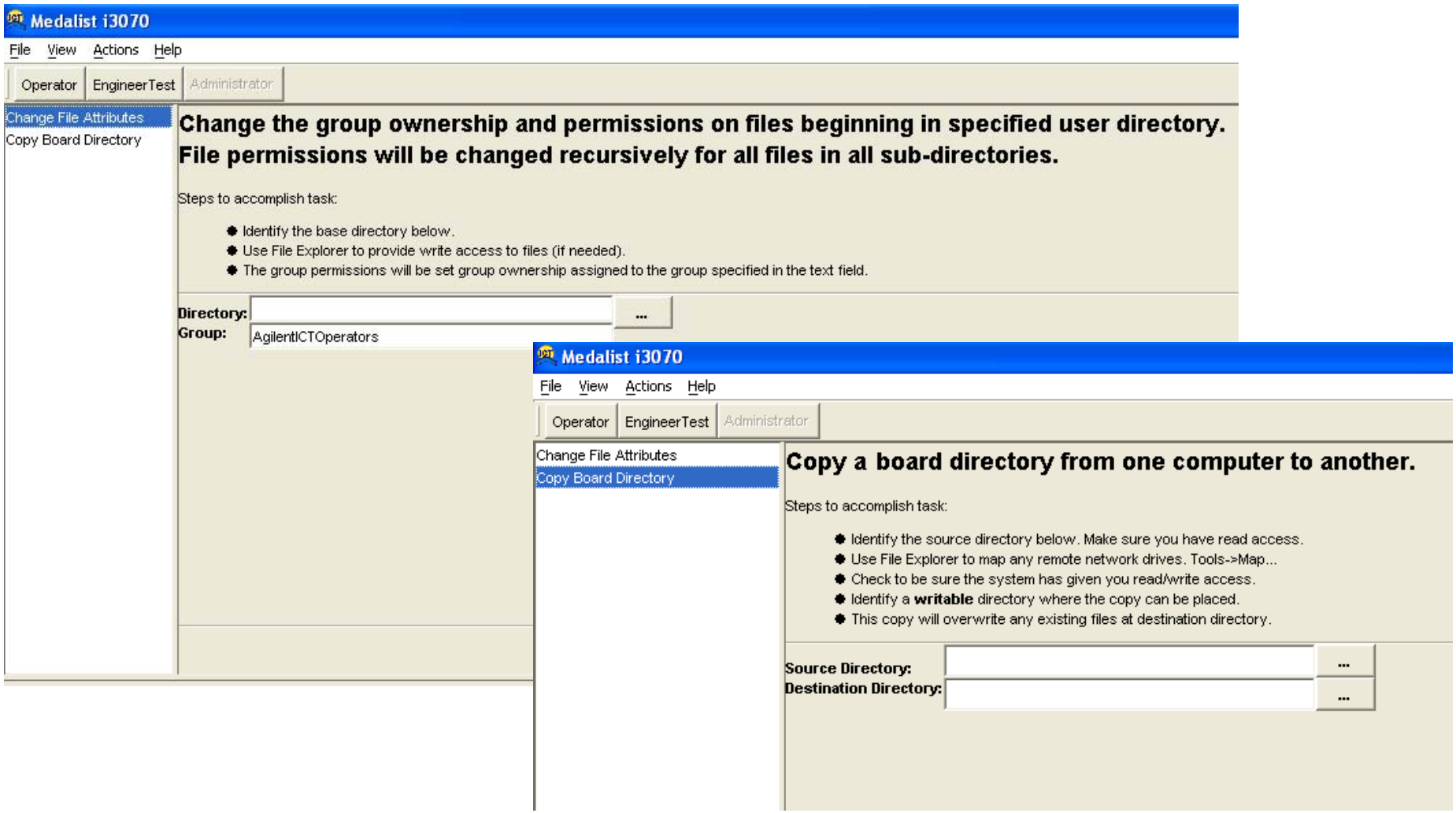


Engineer Login



Graphical User Interface

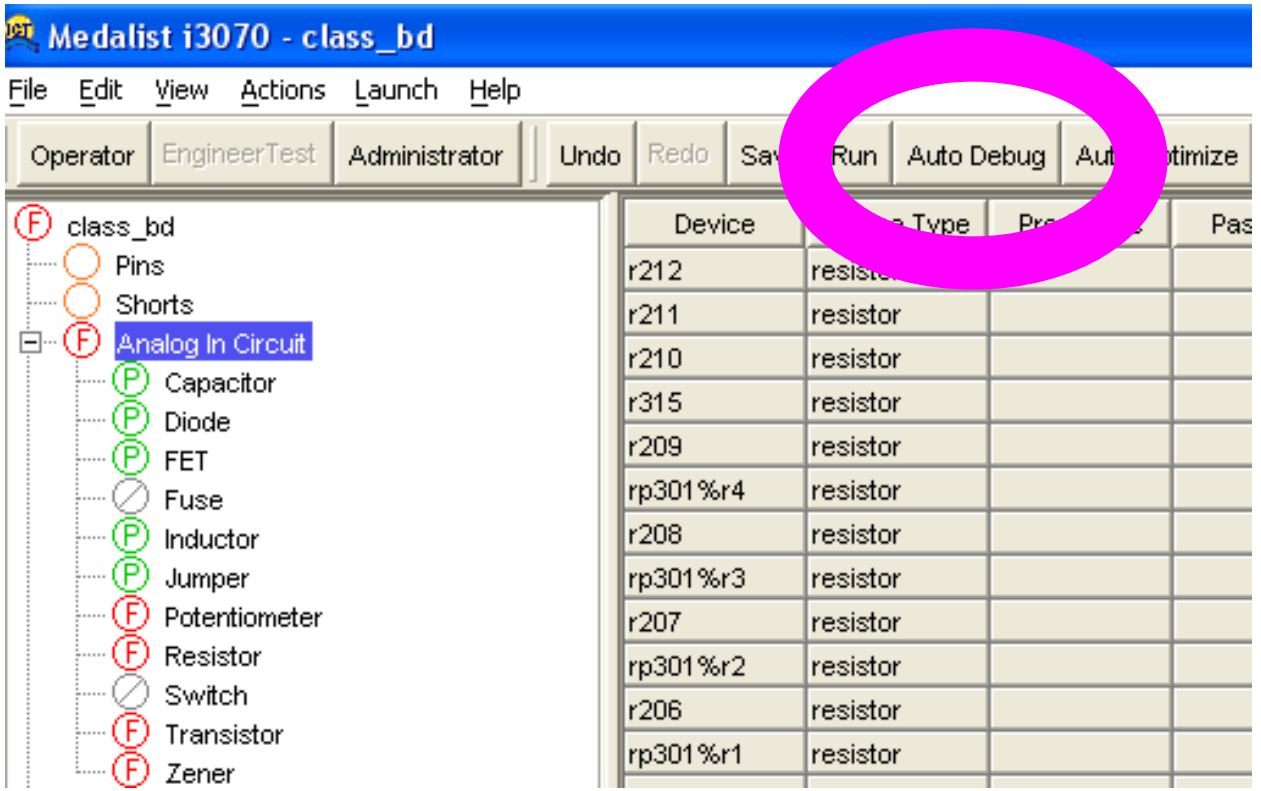
Administrator Login



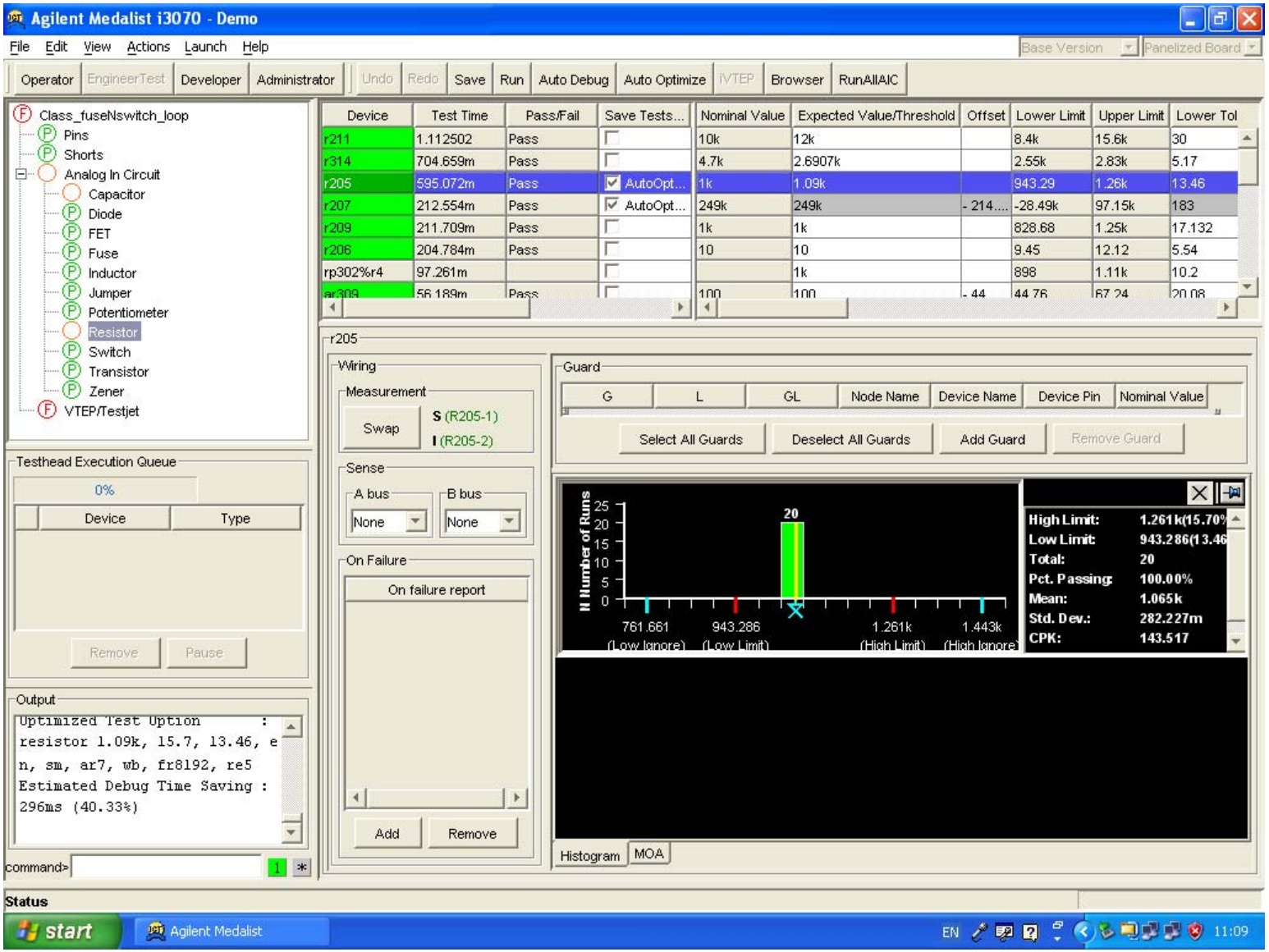
Auto-Debug Interface

Just by a click of a button

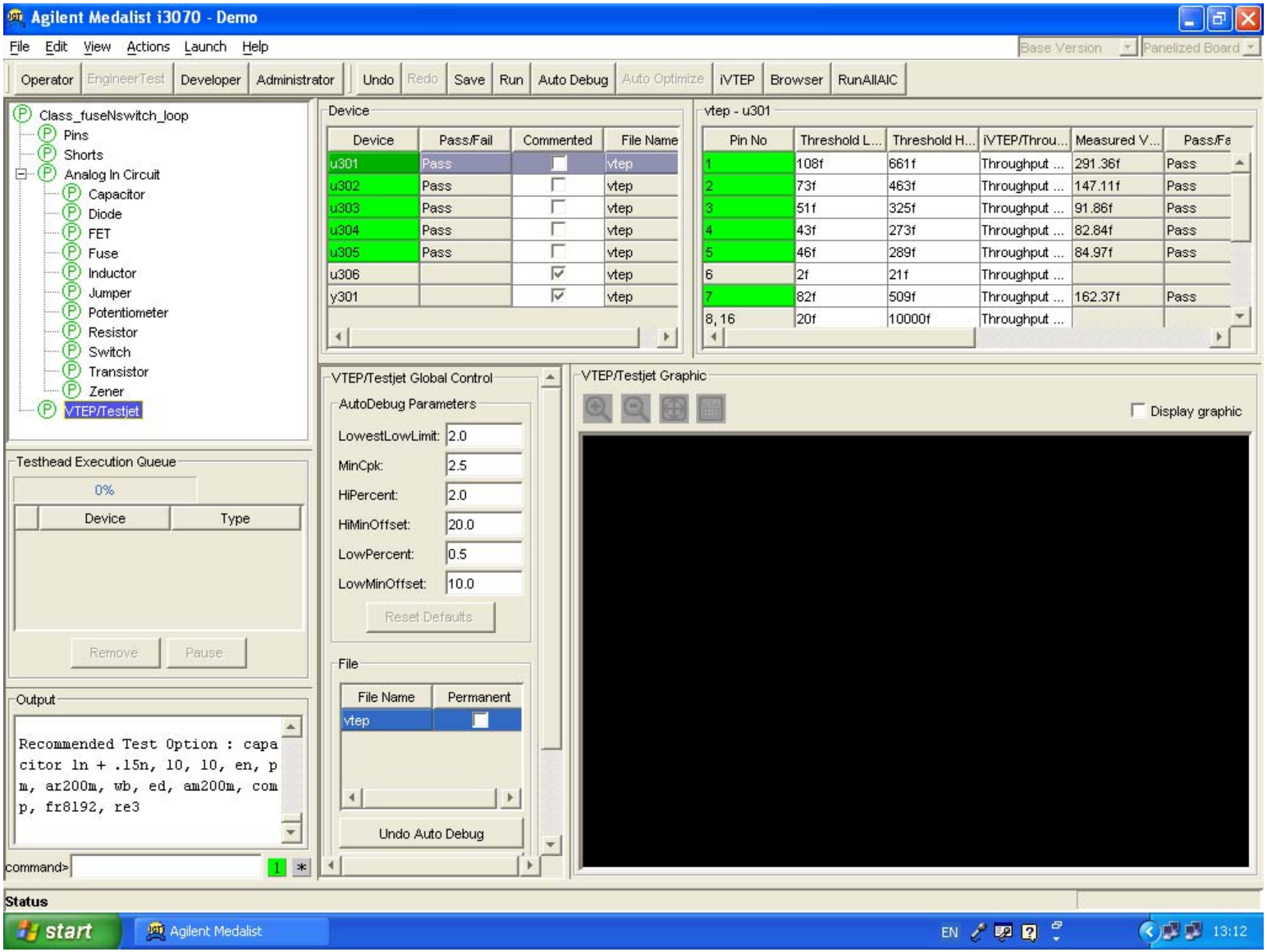
Unpowered Analog Tests will be debugged based on rules that you set.



Auto-Debug Interface



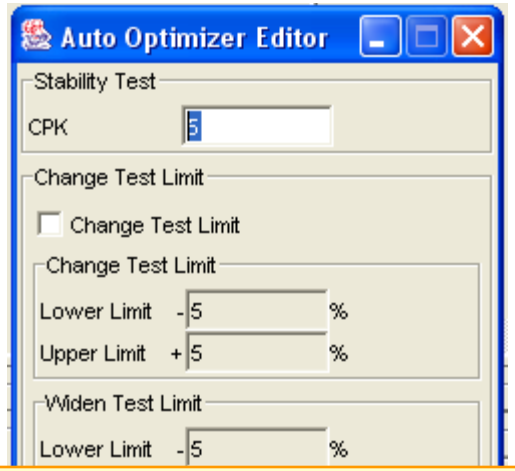
Auto-Debug Interface

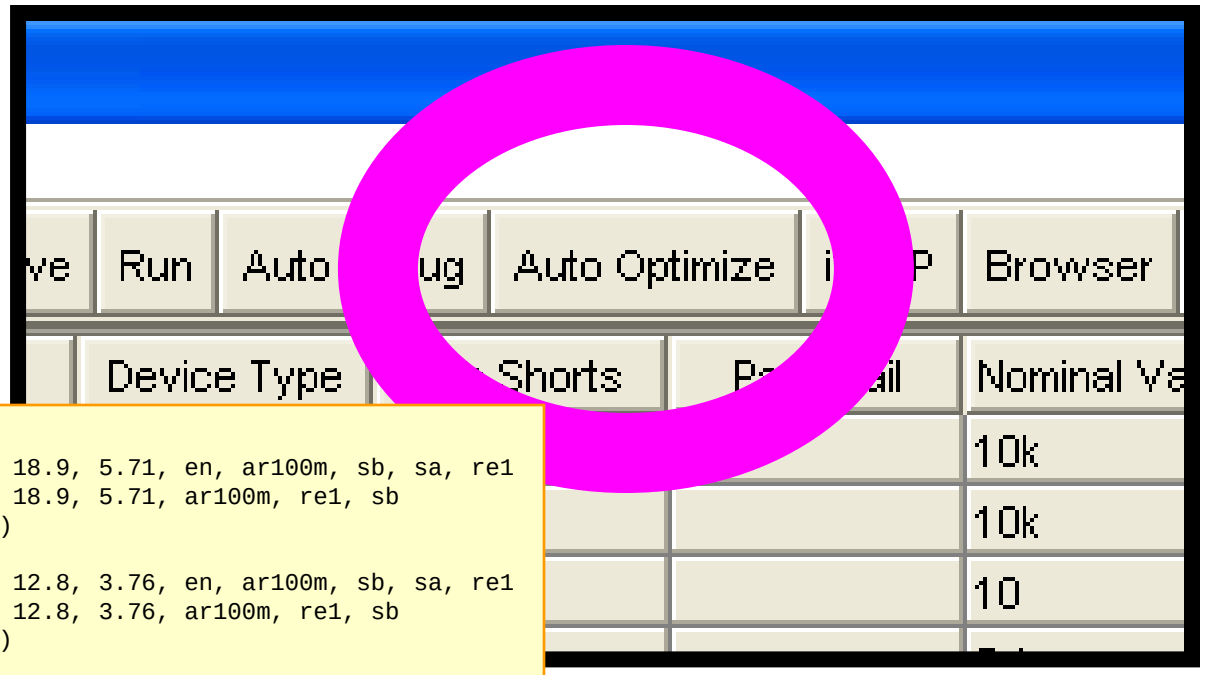


Auto-Optimizer Interface

Just by a click of a button

The Optimizer can save from 10% to 50% of test time per test!

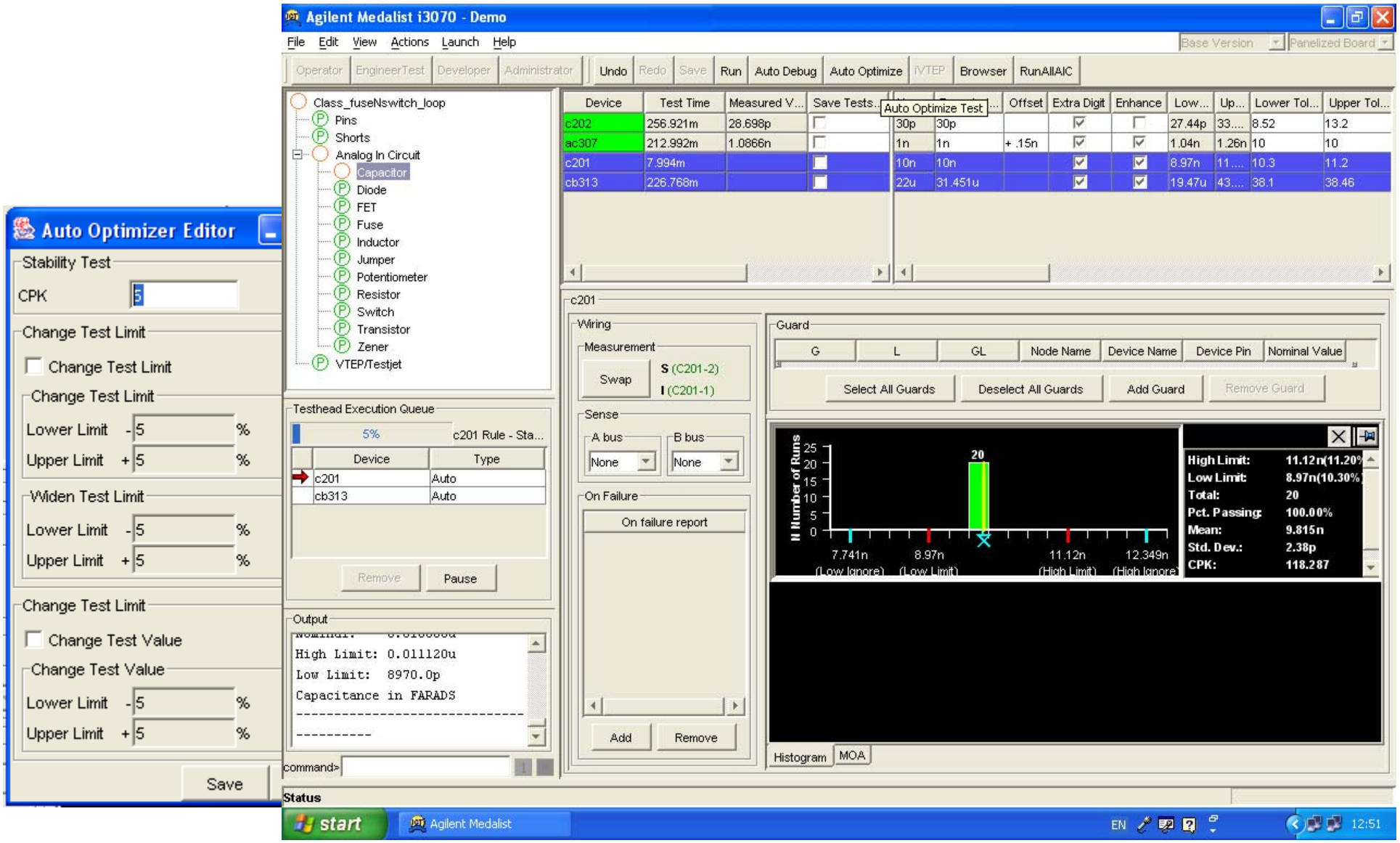




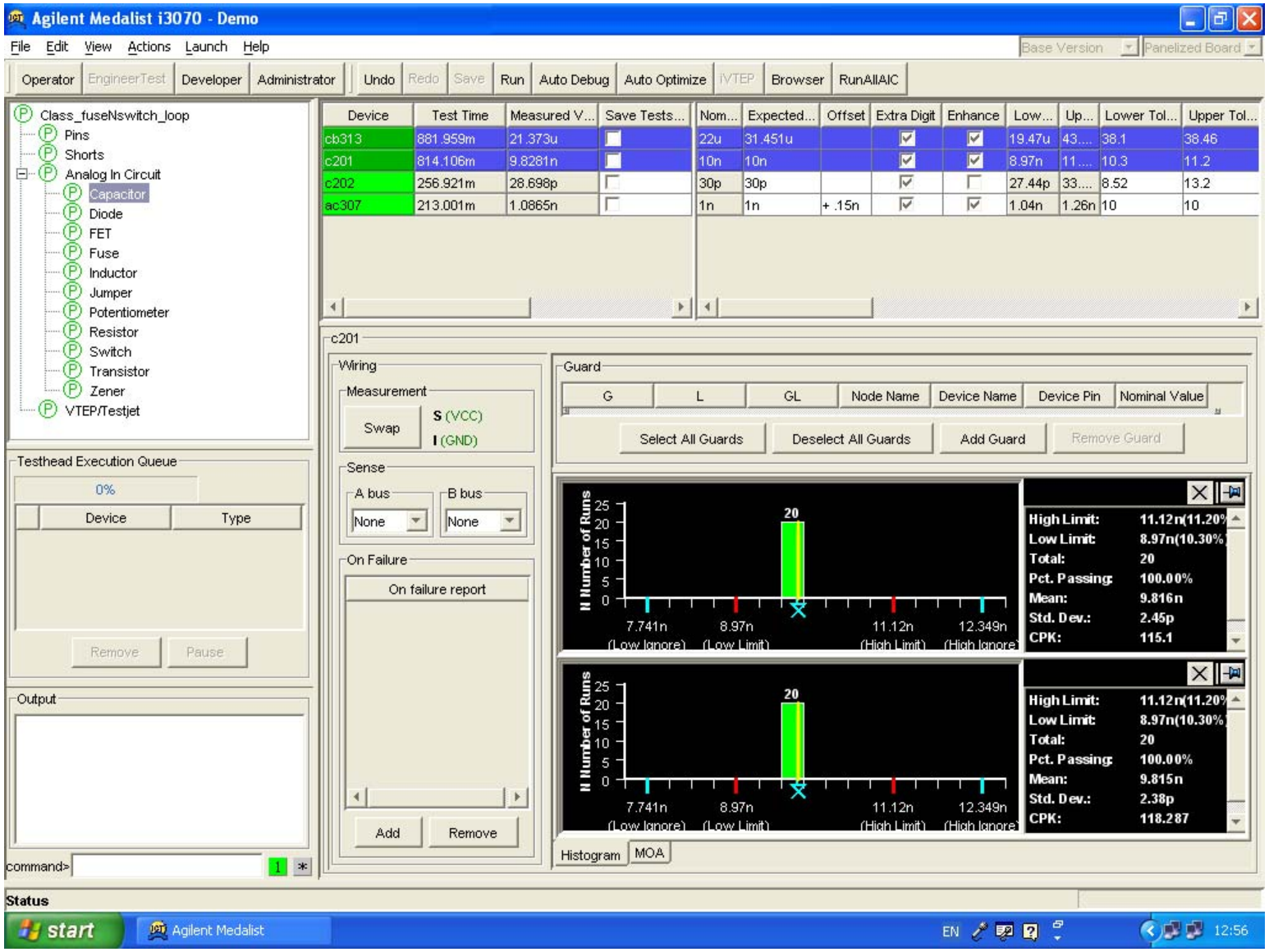

```
Device Name                  : r214
Original Test Option         : resistor 10, 18.9, 5.71, en, ar100m, sb, sa, re1
Optimized Test Option        : resistor 10, 18.9, 5.71, ar100m, re1, sb
Estimated Debug Time Saving  : 31ms (39.74%)
Device Name                  : r210
Original Test Option         : resistor 10, 12.8, 3.76, en, ar100m, sb, sa, re1
Optimized Test Option        : resistor 10, 12.8, 3.76, ar100m, re1, sb
Estimated Debug Time Saving  : 16ms (34.04%)
Device Name                  : r206
Original Test Option         : resistor 10, 12.8, 3.77, en, ar100m, sb, sa, re1
Optimized Test Option        : resistor 10, 12.8, 3.77, ar100m, re1, sb
Estimated Debug Time Saving  : 15ms (24.19%)
```

The Optimiser will only work with Control XTP cards.

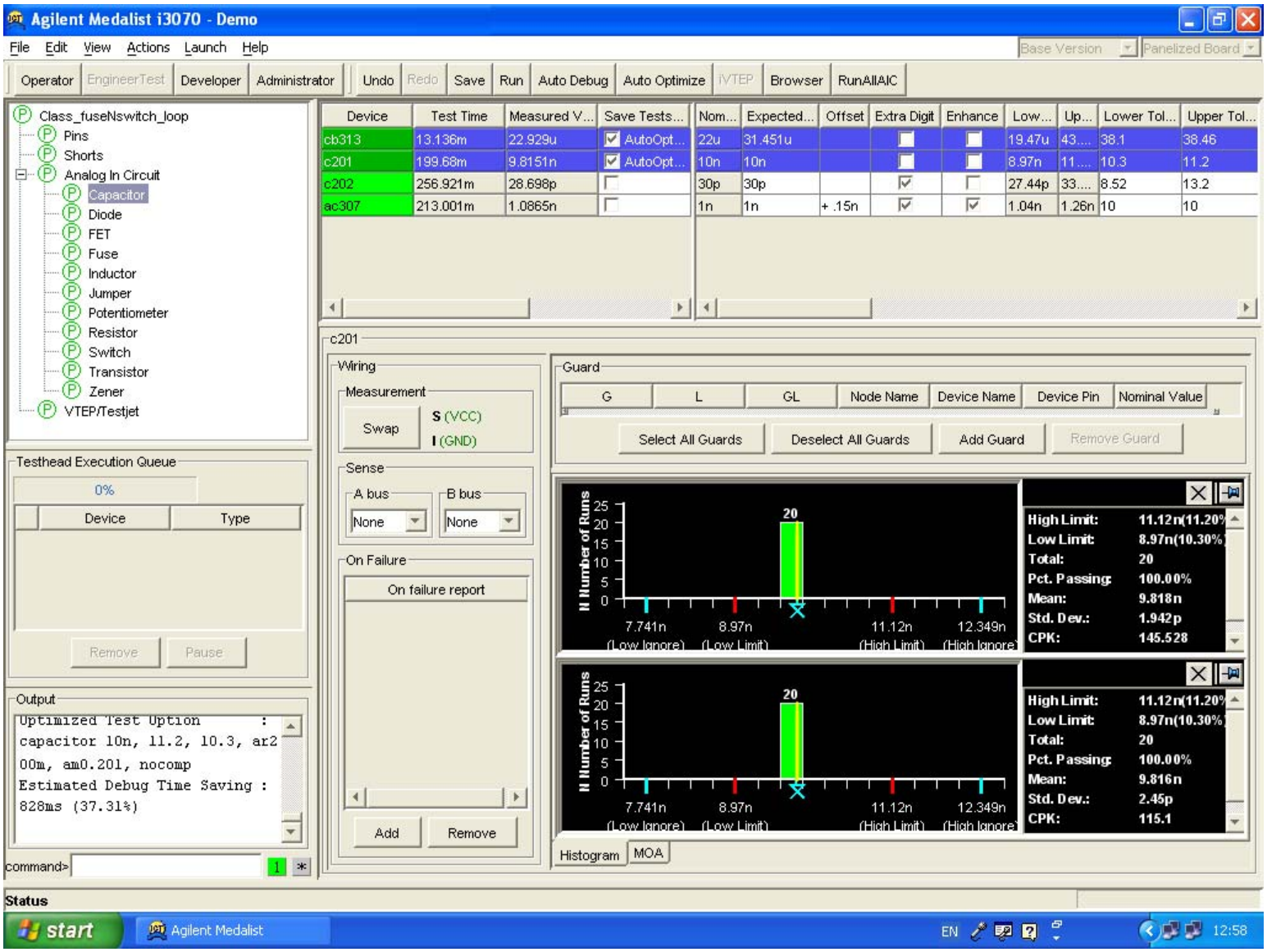
Auto-Optimizer Interface



Auto-Optimizer Interface



Auto-Optimizer Interface



In-Circuit Test Agenda

- New Technology (VTEP 2.0)
- Software Revision 7.0 (i3070) Overview
- Software Revision 7.1 Overview
- Future Releases

i3070 Rev 7.1 Key New Features

New Features

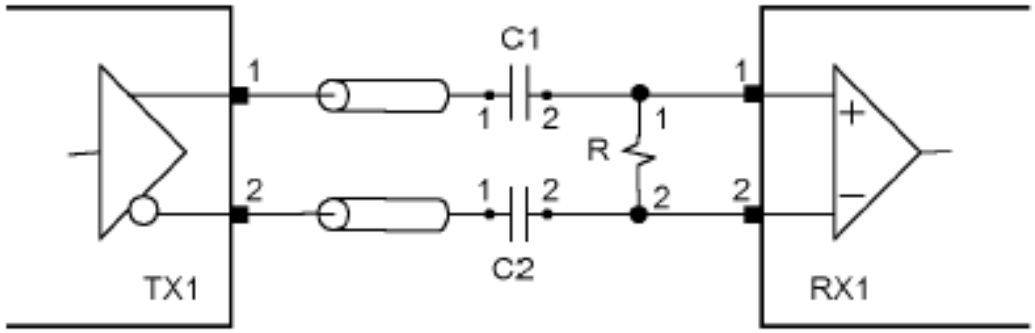
- Native Support for 1149.6 Boundary Scan Standards
- Enhanced Log Records
- Automatic generation of Enhanced FET tests

Enhancements

- VTEP v2.0 test speed up
- NPM libraries for sockets
- auxconnect alternative to fixon

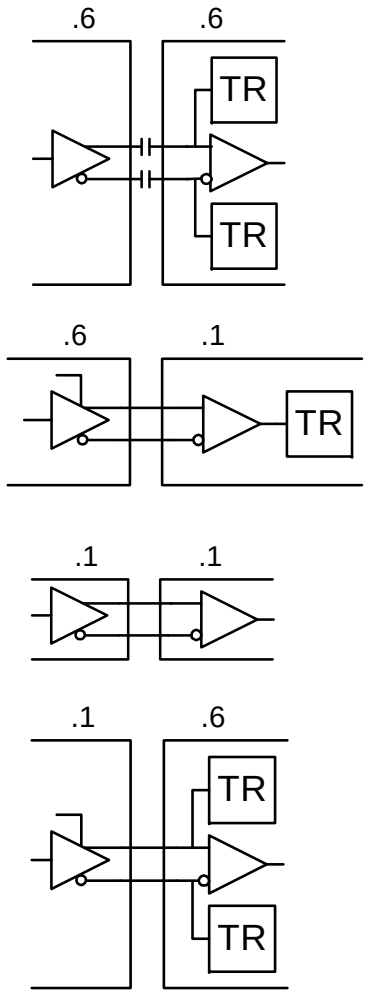
Agilent Medalist 1149.6 Boundary Scan

- Agilent solution to the IEEE 1149.6 Boundary Scan standard
- Industry first native 1149.6 implementation
- To cater for the high speed serial data links
- AC coupling (a series capacitor between driver and receiver)
- Differential signaling
- Offered in ver 07.10p
- No change in use model



Agilent Medalist 1149.6 Boundary Scan

- 1149.6 to 1149.6 AC/DC interconnect tests
- Also adding Differential pair reporting for .1 nets
- 7.1 interconnect Boundary Scan coverage suite is:
  - .6 to .6 AC/DC
  - .6 to .1 DC
  - .1 to .1 DC
  - .1 to .6 DC



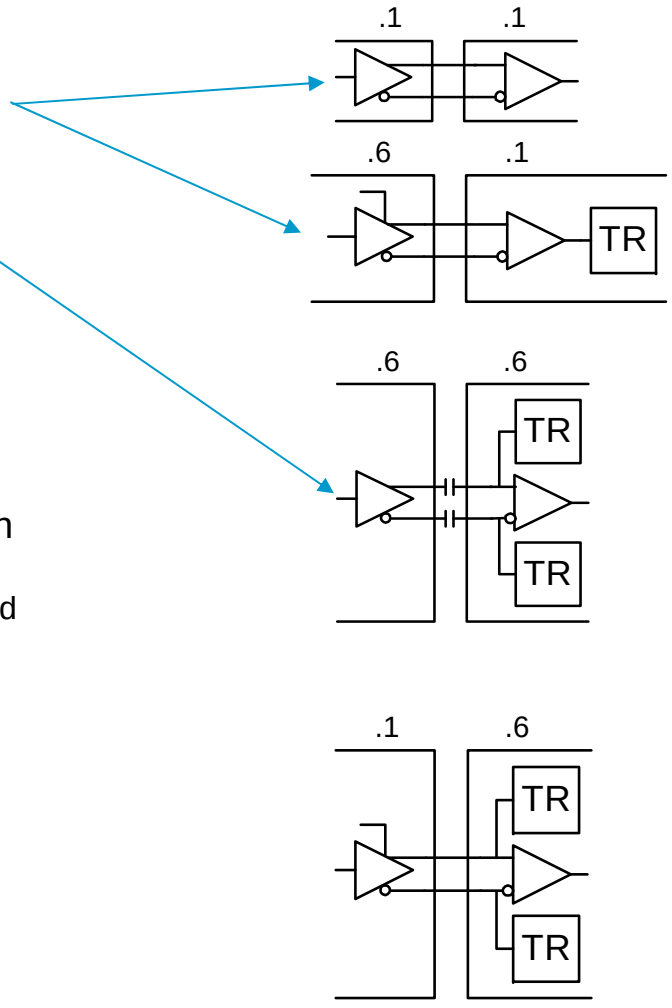
Agilent Medalist i3070 Software Release 7.10p

Two new config enable keywords

- enable advanced boundary scan differential
  - Does not require a new license
- enable 1149.6 boundary scan
  - Requires new 1149.6 Advanced IO license

New ITL test generation enhancements

- u5_u6 (DC only, may be impacted by AC structures)
  - With no new enable keyword, ITL is the same
  - If generated with the “advanced boundary scan differential”
    - Negative legs included and reported on DC-coupled differential structures
- u5_u6_aio (new test for AC and DC structures!)
  - Includes the 1149.6 tests (AC and DC)



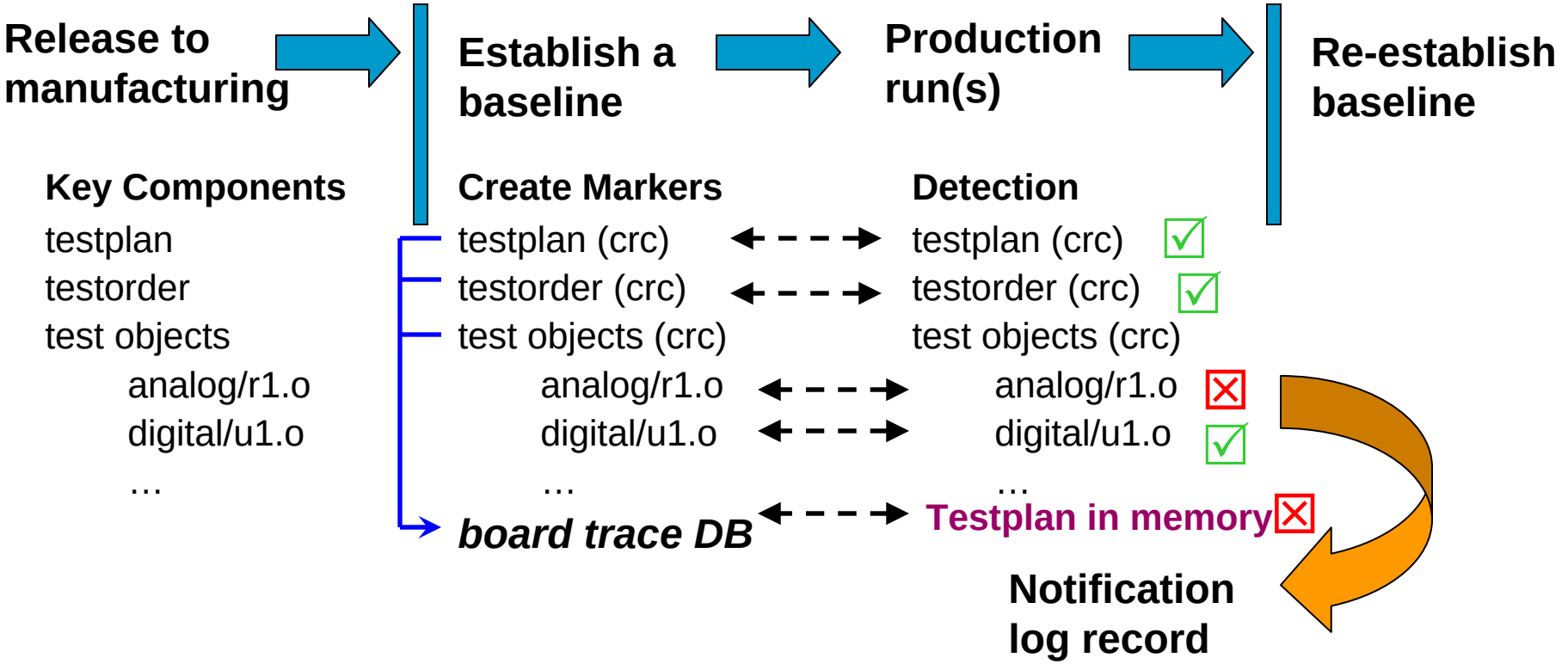
Problem Statement Review

Production board test lacks the tool to detect test program modifications and provide alerts that communicate when such events occur. This results in a loss of coverage and in some case an escapee happens.

The Solution

Test Program Monitoring tool that tracks all the changes in the board directory including object file. A report can be generated that includes the date/time and the file that was changed.

Concept: Integrated Traceability



- Key components are board test elements that are subject to change
- Baseline markers establish a known good working state by storing aside important information
- Detection identifies that a change occurred between a component and its established baseline
- Notification communicates that a changed occurred during a production run

Enhance Log Records Feature

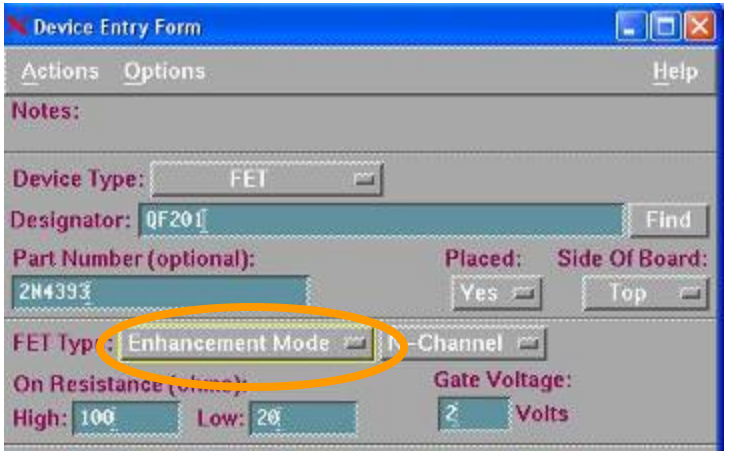
Provide a password mechanism check for controlling the creation/updating a baseline.

- Two passwords provided. One for super-user and one more for a proxy.
- Password creation controlled by a separate application. BT-Basic will not create passwords, only validate them.
- Password encrypted file looked for when baseline command called in BT-Basic.

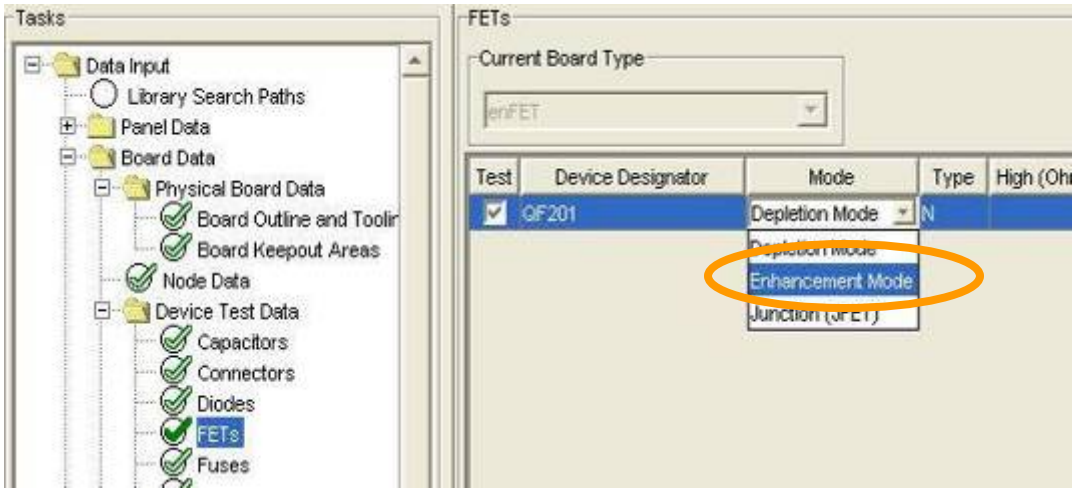
Automated Enhancement FET generation

- The enhancement FET needs gate-source voltage before channel conduct.
- Traditional method is a manual process to create the library for that test.
- This enhancement is to generate a powered analog test for enhancement FET automatically.
- **How to use?**
  - Mux (Board Consultant) and UnMux (Developer - Data-Input)
  - Define the FET type as “Enhancement Mode” and follow the normal development process.

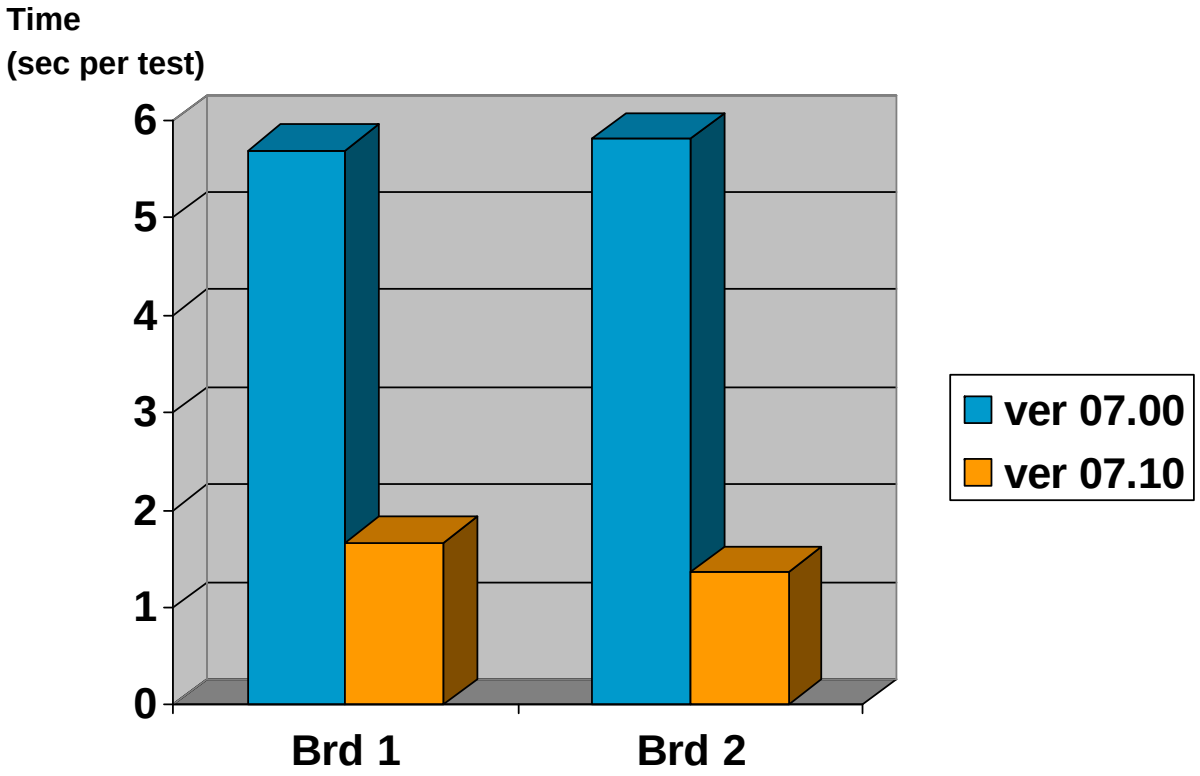
Mux System



UnMux System



VTEP v2.0 Speed Up Results

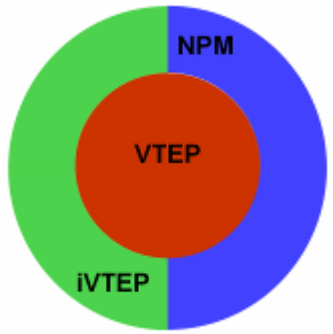


> 4X improvement

	ver 07.00		ver 07.10p	
	Brd#1	Brd#2	Brd#1	Brd#2
Per pin speed (msec)	11	11.3	3.2	2.5
Throughput (pins/sec)	91	89	309	396

Additional Vectorless Test Coverage

VTEP v2.0



- One of the capability of VTEP v2.0 is Network Parameter Measurement.

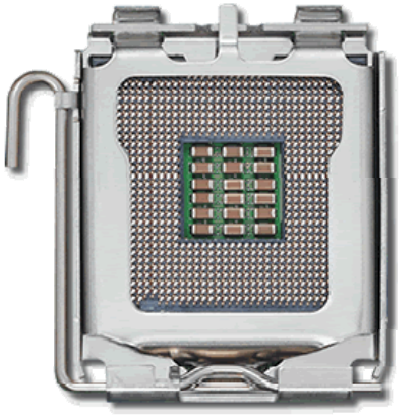
- NPM detects open on PWR and GND pins

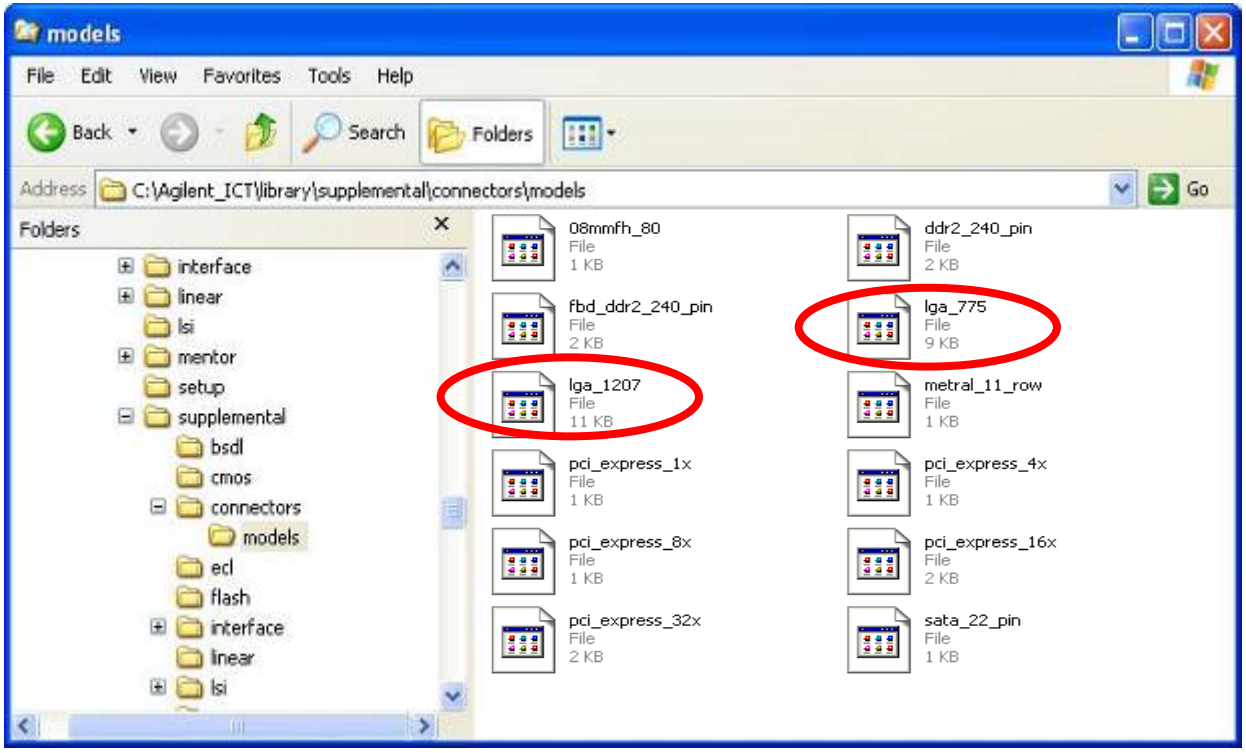
VTEP v2.0	Devices (ICs)	Connectors	Sockets
VTEP			
iVTEP			
NPM			Now  Available!

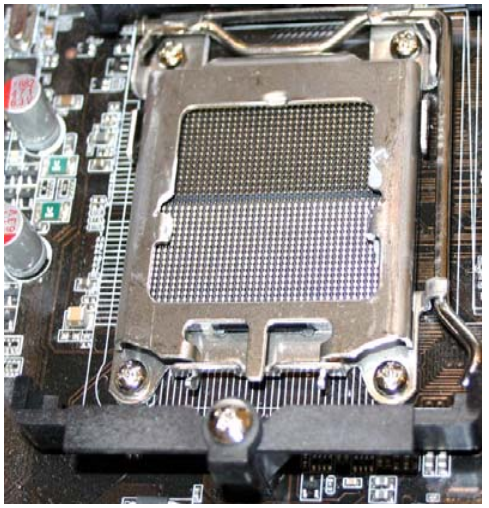
NPM now support CPU sockets

With 7.10p, NPM now supports :

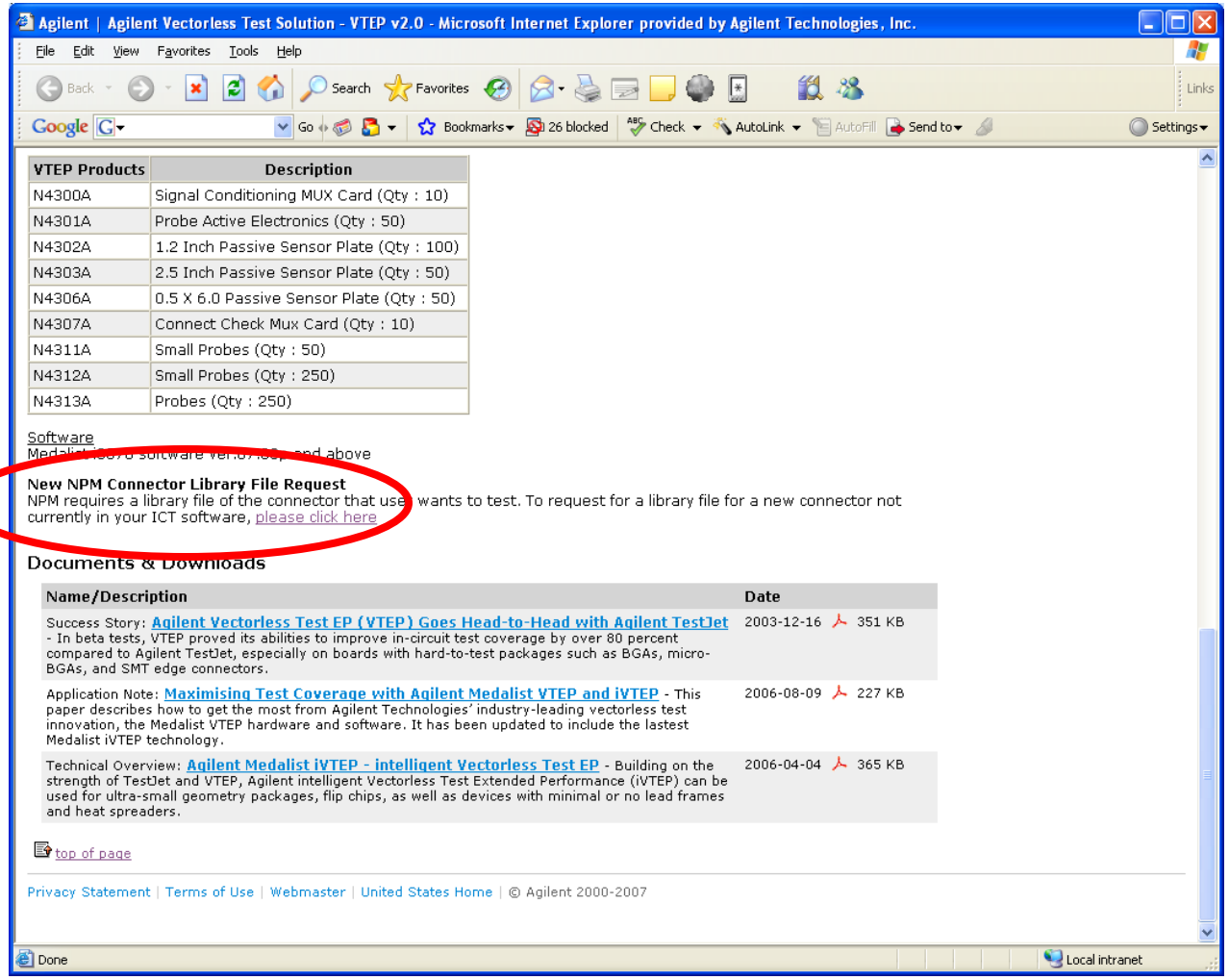
- LGA 775 (Intel based)
- LGA1207 (AMD based)







Requesting new NPM library files



Jumpstations

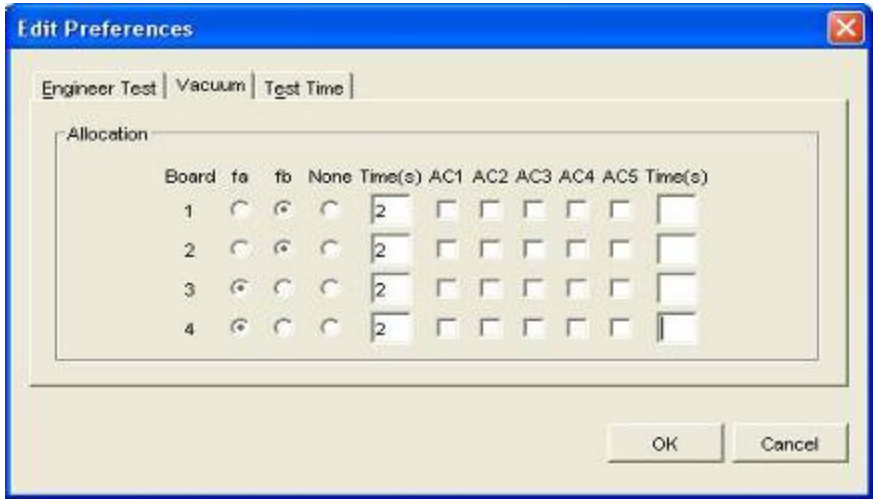
www.agilent.com/see/vtep

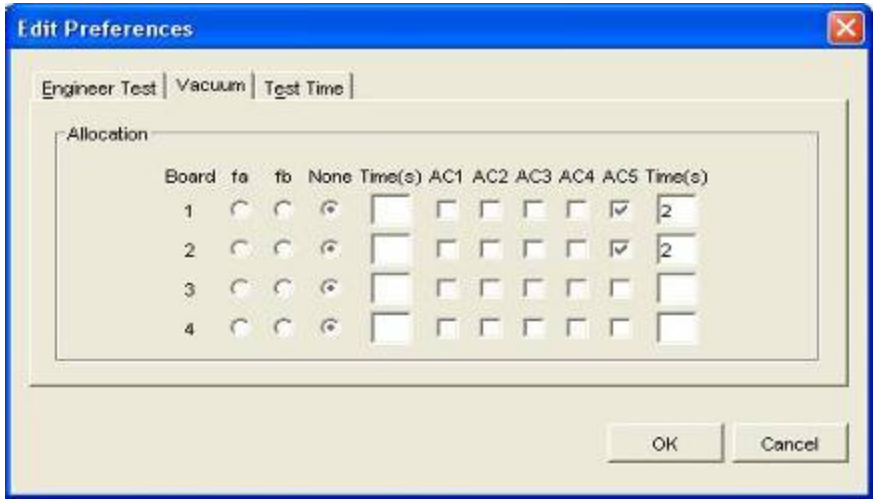
www.agilent.com/see/npm

www.agilent.com/see/ivtep

AUXCONNECT alternative to fxon

- It allows user to use auxconnect as an alternative to fxon.
- How to use it?
- Engineer Test: Edit → Preference → vacuum

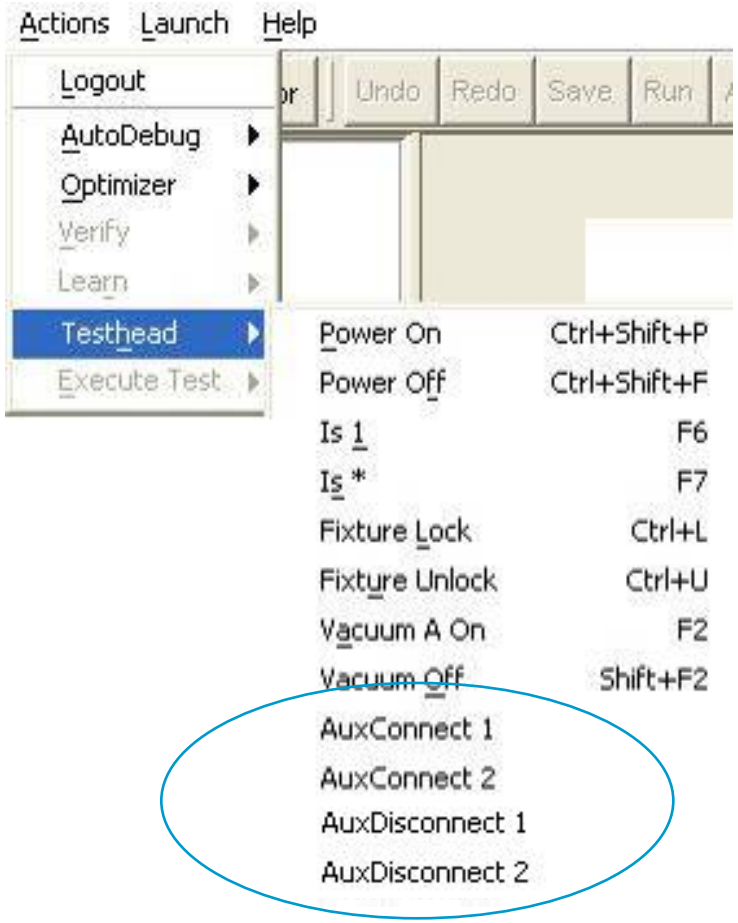




Note: If the relay is defined in the testhead config, auxconnect will not work for that relay.

AUXCONNECT alternative to fxon – Con't

- Pull Down Menu to activate: Actions → Testhead



Future Releases

Software Releases 2008

- Thruput improvements
- Digital Drive Thru
- Serial Bus Support (I2C, SPI)
- Additional Limited Access Technology

Web Links


Agilent
3070 Series 3
In-circuit Test
Agilent
3070 Series 3
In-circuit Test

Useful Web Links

Software Updates Information –

http://www.home.agilent.com/agilent/facet.jspx?t=80045.k.1&co=152910.i.2&cc=US&lc=eng&sm=g

VTEP & iVTEP Information –

http://www.home.agilent.com/USeng/nav/-536900456.0/pc.html

Hardware and Software Support Details -

http://www.agilent.com/see/support

ISP Flash/PLD –

http://www.home.agilent.com/USeng/nav/-536900451.0/pc.html

Bead Probe –

http://www.agilent.com/see/beadprobe